AC-DC CONVERTER

NOVEL METHODOLOGY OF AC - DC SOLID STATES VALLEY FILLS WITH POWER FACTOR CORRECTION

Point out of AC direct DC conversion with full bridge diode rectifies problems

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UNDESIRABLE RIPPLE

While half-wave and full-wave rectification can deliver unidirectional current, neither produces a constant voltage.

Producing steady DC from a rectified AC supply requires a smoothing circuit or filter.
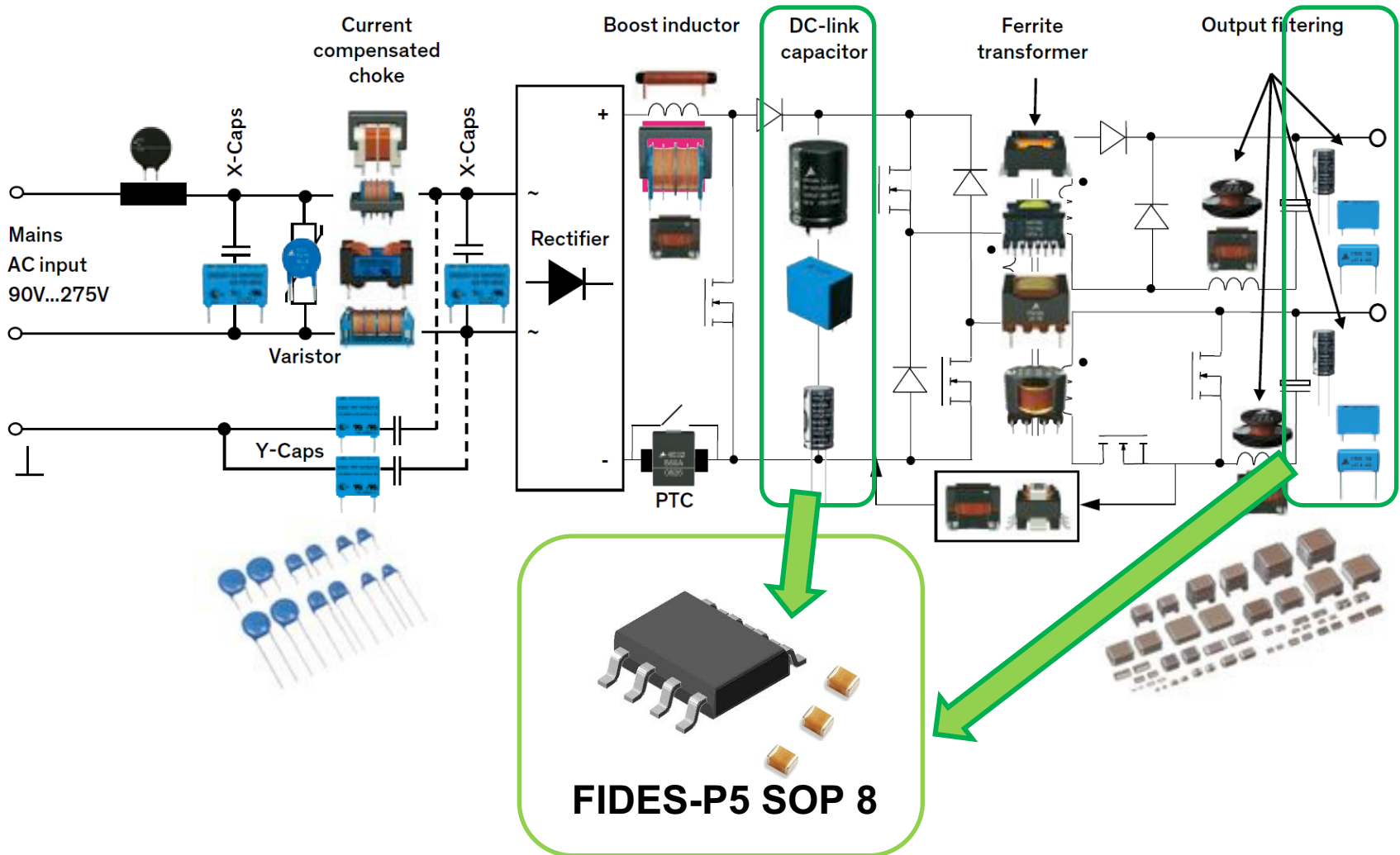
In its simplest form this can be just a reservoir capacitor or smoothing capacitor, placed at the DC output of the rectifier.

There is still an AC ripple voltage component at the power supply frequency for a half-wave rectifier, twice that for full-wave, where the voltage is not completely smoothed.
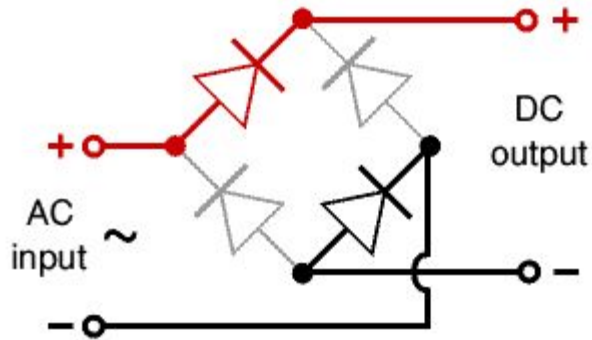
Electrolytic capacitors can evaporate through a temperature-dependent drying-out process, which causes electrical parameters to drift, limiting the service life time of the capacitors.

High-amplitude ripple currents shorten the life of electrolytic capacitors.

SMPS CAPACITOR PARTS SUBSTITUTION

Current compensated choke

Boost inductor

DC-link capacitor

Ferrite transformer

Output filtering

X-Caps

X-Caps

Mains AC input 90V...275V

Rectifier

Varistor

Y-Caps

PTC

FIDES-P5 SOP 8

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WHAT IS PROBLEMS OF AC-DC CONVERSION

DC output

AC input ~

Bridge rectifier

Alternate pairs of diodes conduct, changing over the connections so the alternating directions of AC are converted to the one direction of DC.

current or voltage

time
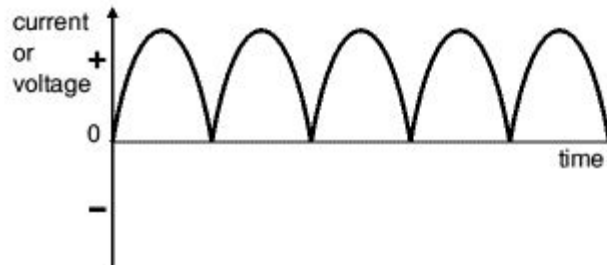
Output: full-wave varying DC
(using all the AC wave)

1. When AC to DC must be come to current zero point.
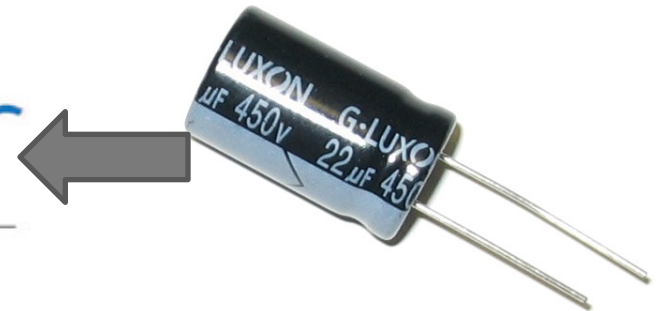2. Dammed high current by capacitor.
3. The Electrolytic capacitor

AC voltage coming from the transformer is a sine wave.
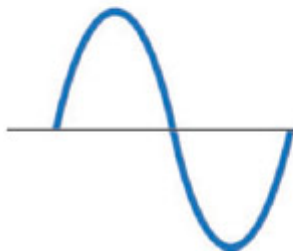
The rectifier tube flips half of the wave to create a DC ripple.

The filter capacitors help smooth out the ripple.

LUXON G-LUXO
µF 450v   22 µF 45

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MOVE OVER TO DIGITAL CONTROLLED SOLID CAPACITOR

Substitution

FIDES-P5 SOP 8

MTBF OVER 100K hours sustainable life cycles

Elrctolytic capacitors service life problem

T_0: Operating temperature [℃]

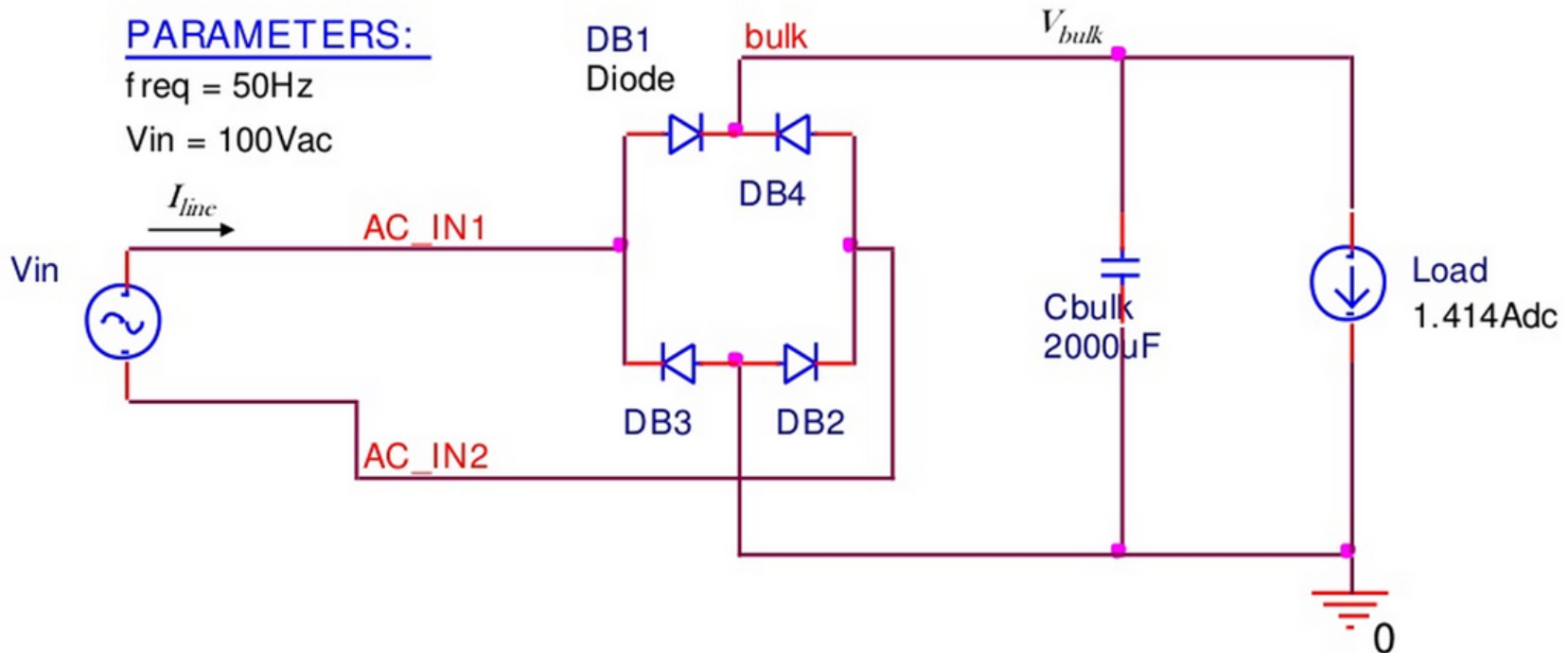$$L = L_0 \times 2^{\frac{T - T_0}{10}}$$

L: Expected service life [hrs]
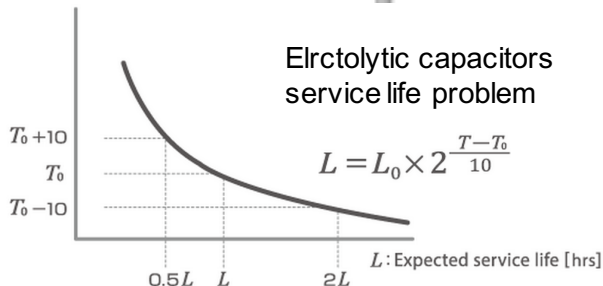
For every rise in operating temperature by 10 degrees centigrade, the service life is shortened to one half, and double for every 10 degree drop(10 degree 2 fold rule). The aluminum electrolytic capacitor is commonly 10 years service life)

Benefit :
1. Long life MTBF
2. Good PFC (over 0.95)
3. Stable operating temperature
4. Small size

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AC-DC CONVERSION

PARAMETERS:
freq = 50Hz
Vin = 100Vac

I_{line}

Vin

AC_IN1

AC_IN2

DB1
Diode

DB4

DB3   DB2
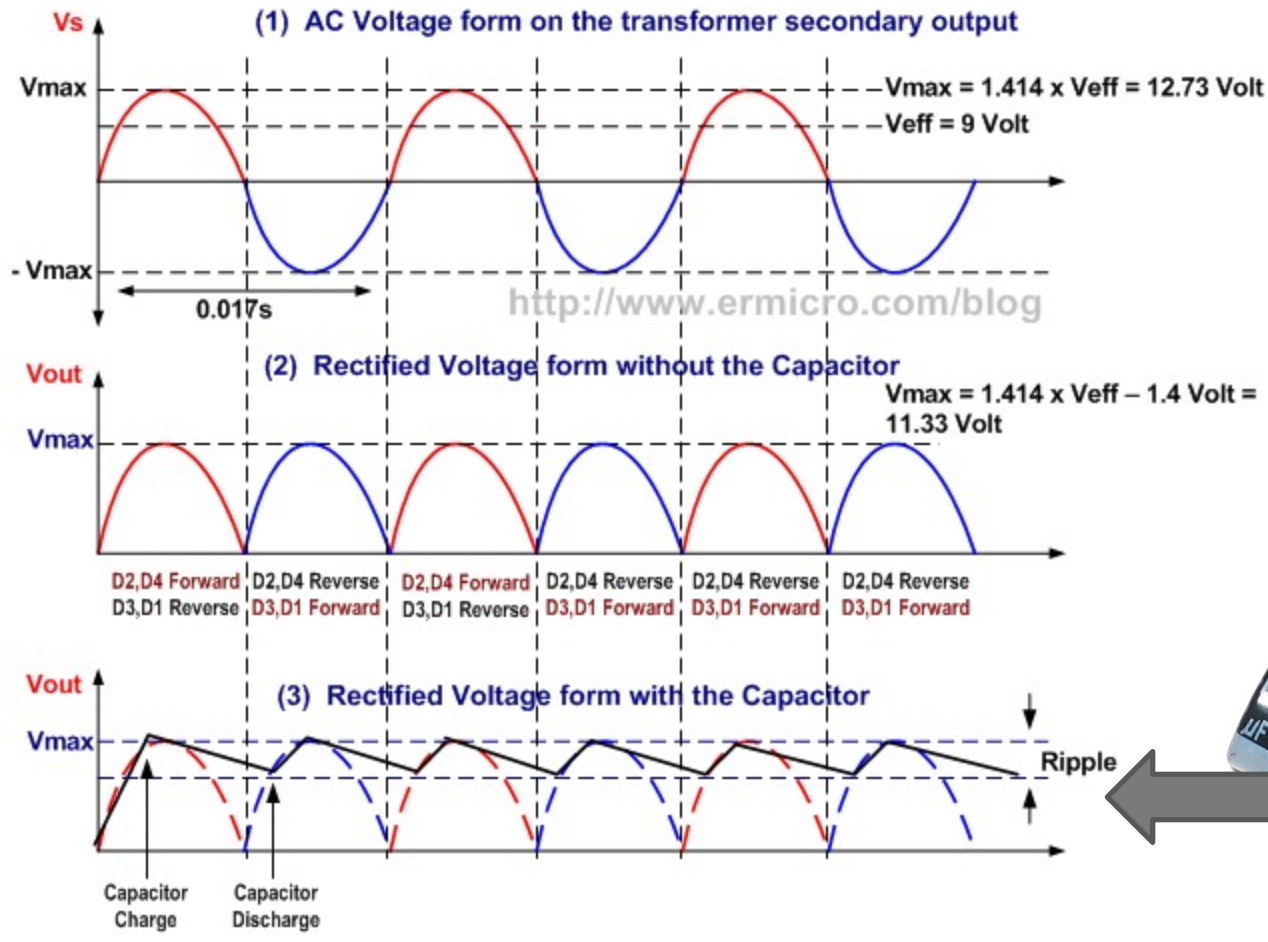
bulk

V_{bulk}

Cbulk
2000uF

Load
1.414Adc

0

Most electronic ballasts and switching power supplies use a bridge rectifier and bulk storage capacitor to derive raw DC voltage from the utility AC line.
Figure above: Vin=100Vac, 60Hz and Po=200W.

BRIDGE RECTIFYING POWER FACTOR
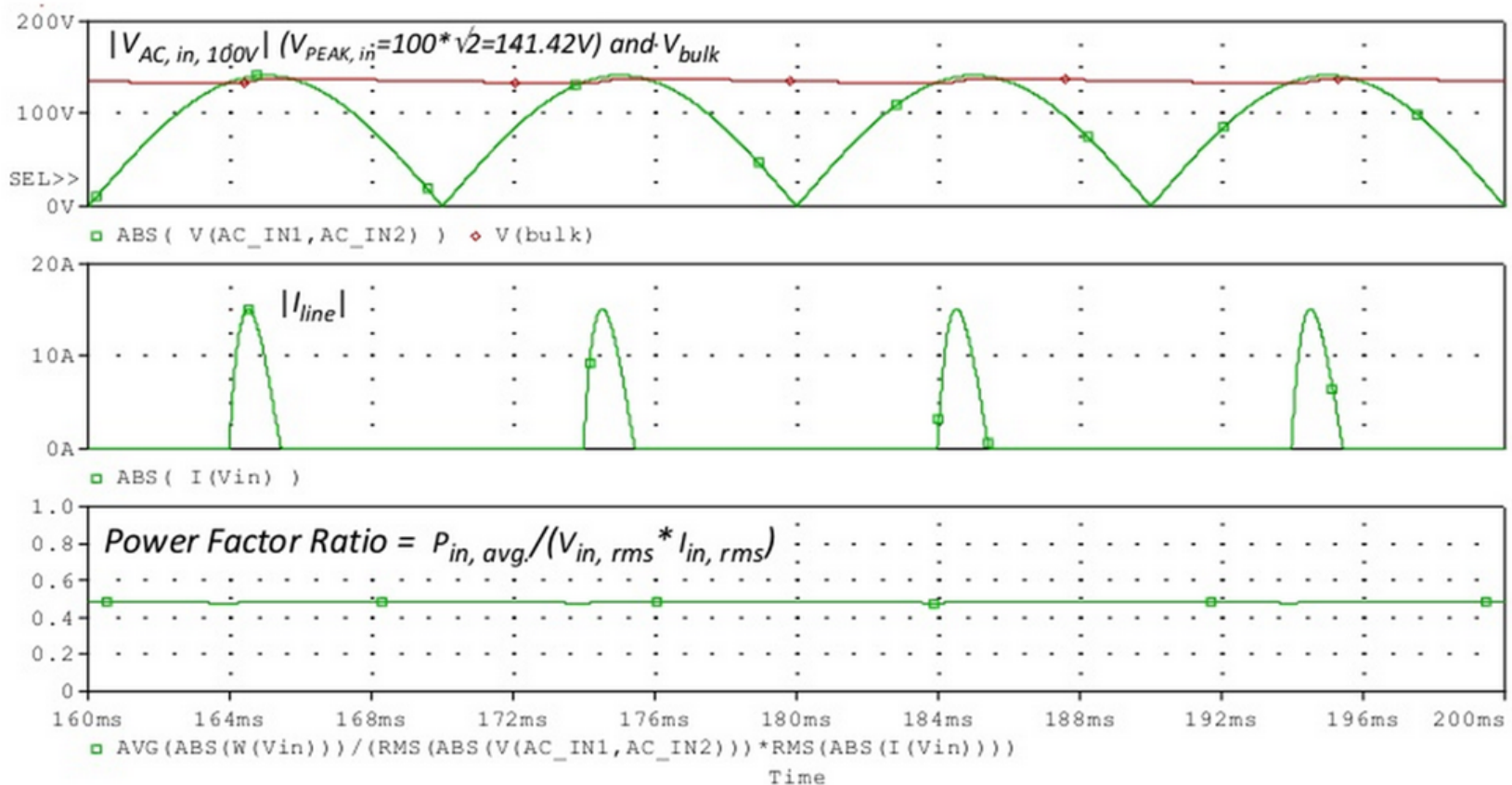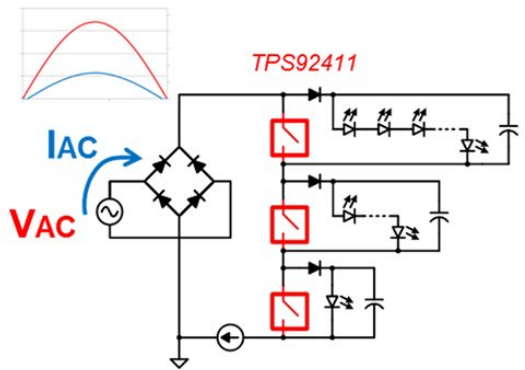

The uncorrected power factor rectifying circuit draws current from the AC lin when the AC voltage exceeds the capacitor voltage(Vbulk). The current(Iline) is non-sinusoidal. This results in a poor power factor condition where the apparent input power is much higher then real power, figure above, power factor ratios of 0.5 to 0.7 are common.

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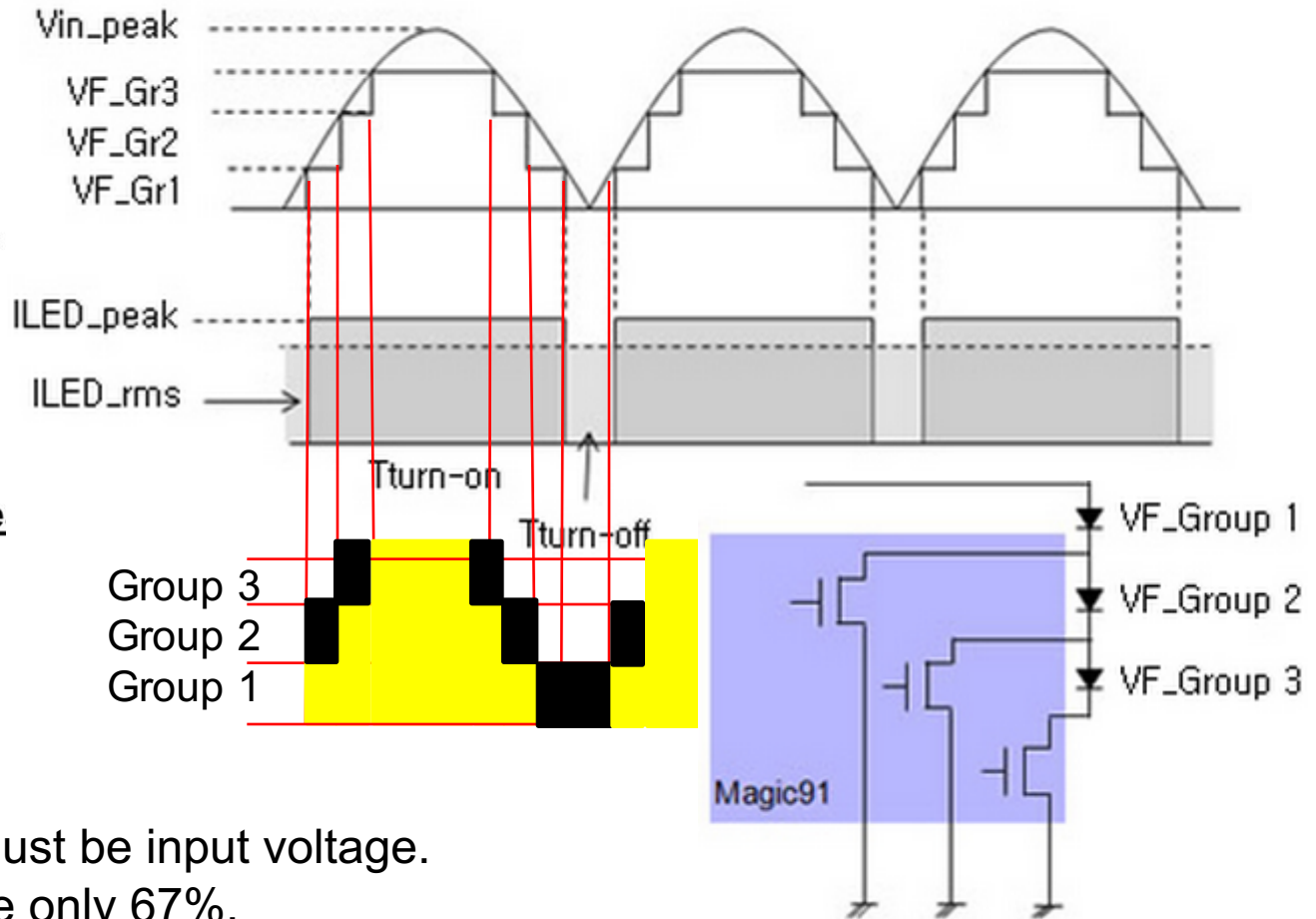
AC-DC RECTIFIER

(1) AC Voltage form on the transformer secondary output

Vmax = 1.414 x Veff = 12.73 Volt
Veff = 9 Volt

0.017s

http://www.ermicro.com/blog

(2) Rectified Voltage form without the Capacitor

Vmax = 1.414 x Veff − 1.4 Volt = 11.33 Volt

| D2,D4 Forward | D2,D4 Reverse | D2,D4 Forward | D2,D4 Reverse | D2,D4 Reverse | D2,D4 Reverse |
| D3,D1 Reverse | D3,D1 Forward | D3,D1 Reverse | D3,D1 Forward | D3,D1 Forward | D3,D1 Forward |

(3) Rectified Voltage form with the Capacitor

Ripple

Capacitor Charge

Capacitor Discharge

The AC to DC full wave rectifier Voltage time diagram

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AC DIRECT LED DRIVER PROBLEM DEMYSTIFIED

TPS92411 Switched Line

Vin_peak
VF_Gr3
VF_Gr2
VF_Gr1

ILED_peak
ILED_rms

Tturn-on
Tturn-off

Group 3
Group 2
Group 1

VF_Group 1
VF_Group 2
VF_Group 3

Magic91

Demerit
1. Need LED Vf must be input voltage.
2. LED on time are only 67%.
3. LED string group illumination are not same.

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NON ISOLATION BUCK LED DRIVER

Most of LED driver are employed.
Poor PFC and ripple.
Electolytic ca

FL7701

DSG: Digital Sine-Wave Generator
HV Device : High-Voltage Device

Ripple reduce

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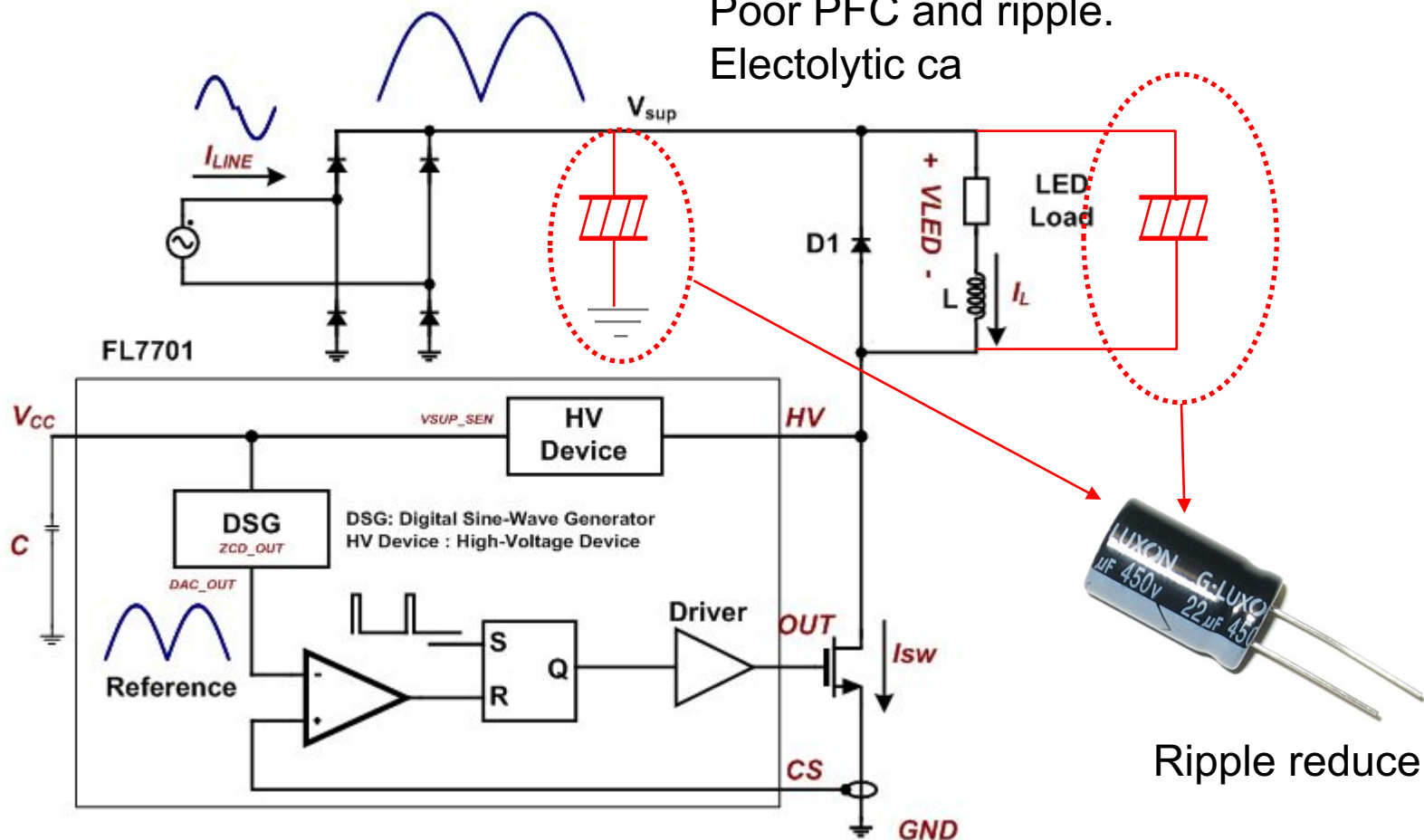
RIPPLE AND PFC PROBLEM

Figure. A
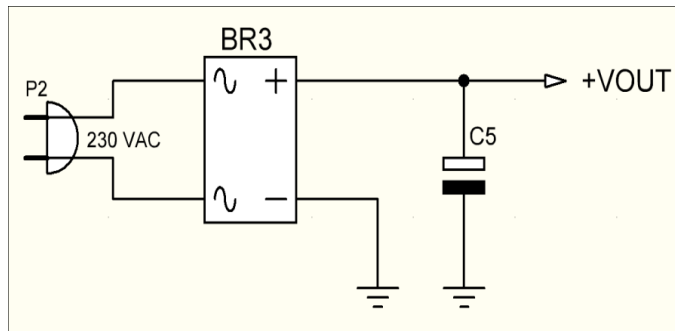
Figure. B
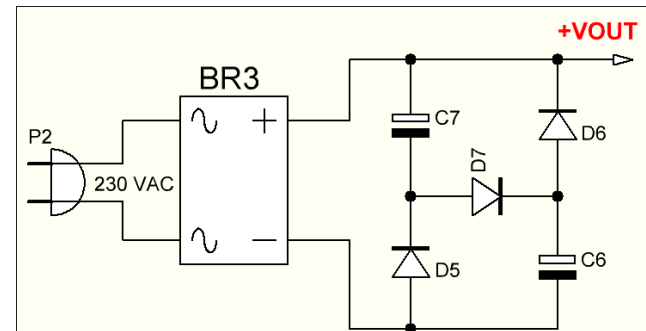
Figure. C
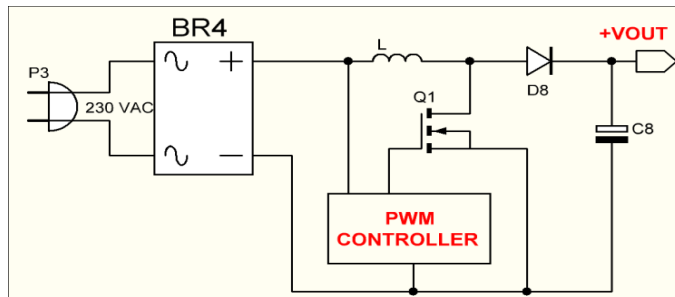
Figure. D
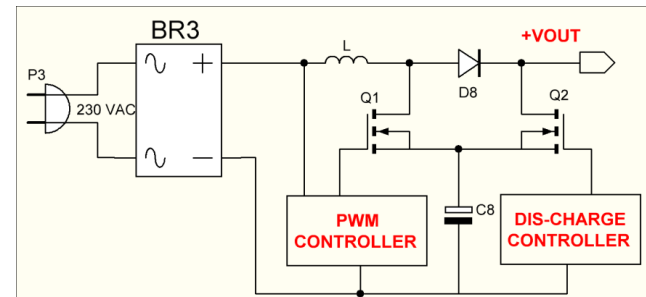
Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw dc voltage from the utility a line, figure above : valley fill with passive PFC circuits B and active PFC shown C. The figure D are this novel PFC and regulation methodology.
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ADVANTAGES - DISADVANTAGES OF VALLEY FILL PASSIVE PFC

Passive power factor correctors have certain advantages, such as
- Simplicity
- Reliability
- Ruggedness
- Insensitive to noise and surges
- No generation of high-frequency EMI
- No high frequency switching losses

Cockcroft-Walton PFC

Disadvantages of passive PFC
On the other hand, they also several drawbacks
- Solutions based on filters are heavy and bulky because line frequency reactive components are used
- They have poor dynamic response
- Lack voltage regulation and the shape of their input current depend on the load
Even though line current harmonics are reduced, the fundamental component may show an excessive phase shift that reduces the power factor
- Parallel resonance at different frequencies occurs too, which can amplify other harmonic
- Big size and expensive

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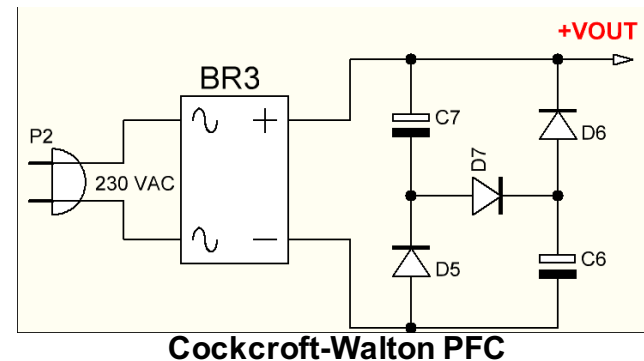
HV9910 PASSIVE POWER FACTOR BUCK LED DRIVER

The purpose of the valley-fill circuit (see Figure 1) is to allow the buck converter to pull power directly off the AC line when the line voltage is greater than 50 percent of its peak voltage. The following equation shows the maximum bus voltage at the input of the buck converter:

$$V_{IN(max)} = \sqrt{2} \times V_{ac(max)} = \sqrt{2} \times 264 Vac = 373\ V$$

During this time, capacitors within the valley-fill circuit (C1 and C2) are in series and charged via D2 and R1. If the capacitors have identical capacitance value, the peak voltage across C1 and C2 is $V_{IN(max)}$ /2 = 186 V. Often, a 20 percent difference in capacitance can be observed between like capacitors. Therefore, a voltage rating margin of 25 percent should be considered. Once the line drops below 50 percent of its peak voltage, the two capacitors are essentially placed in parallel. The bus voltage $V_{IN(min)}$ is the lowest voltage value at the input of the buck converter. $V_{IN(min)}$ at the minimum AC line voltage $V_{ac(min)}$ is as follows:

$$V_{IN(min)} = \sqrt{2} \times \frac{V_{ac(min)}}{2} = \sqrt{2} \times \frac{85 Vac}{2} = 60\ V$$

At 60 Hz, the total time of a half AC line cycle is 8.33 ms. The power to the buck converter is derived from the valley-fill capacitors when the AC line voltage is equal to or less than 50 percent of its peak voltage. The holdup time for the capacitors equates to t_{HOLD} = 1/3 x 8.33 ms = 2.77 ms. The valley-fill capacitor value can then be calculated with the following equation:
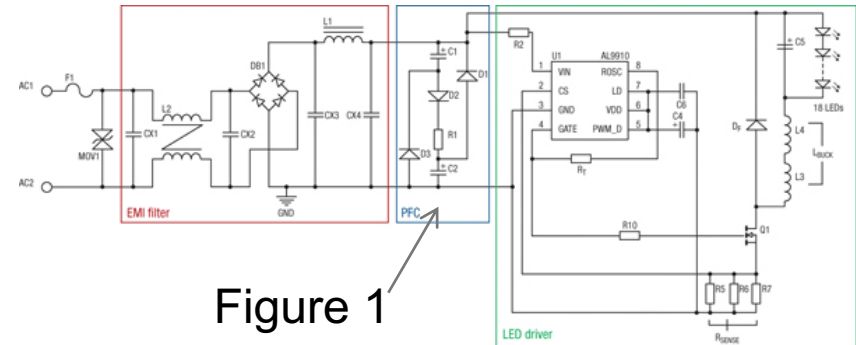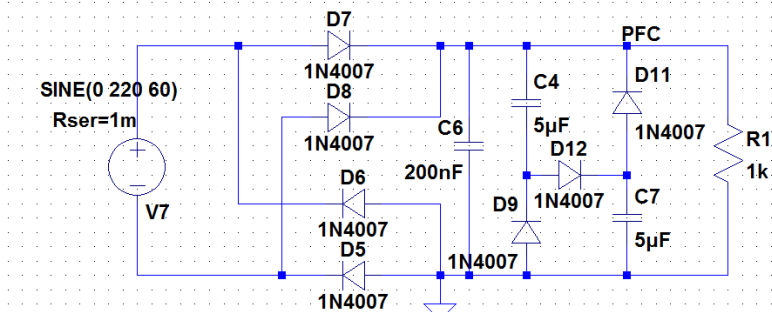

Figure 1
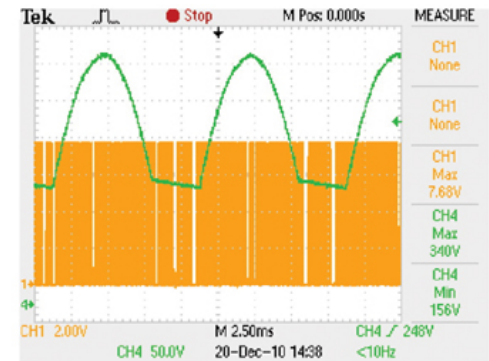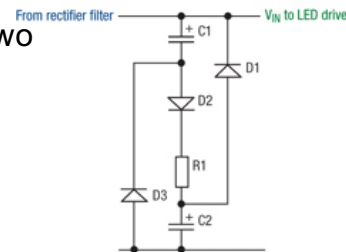
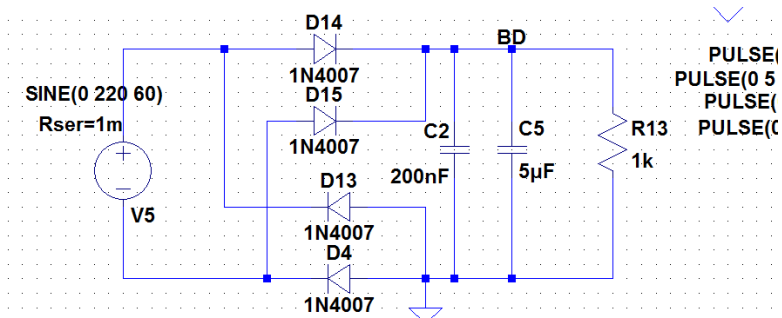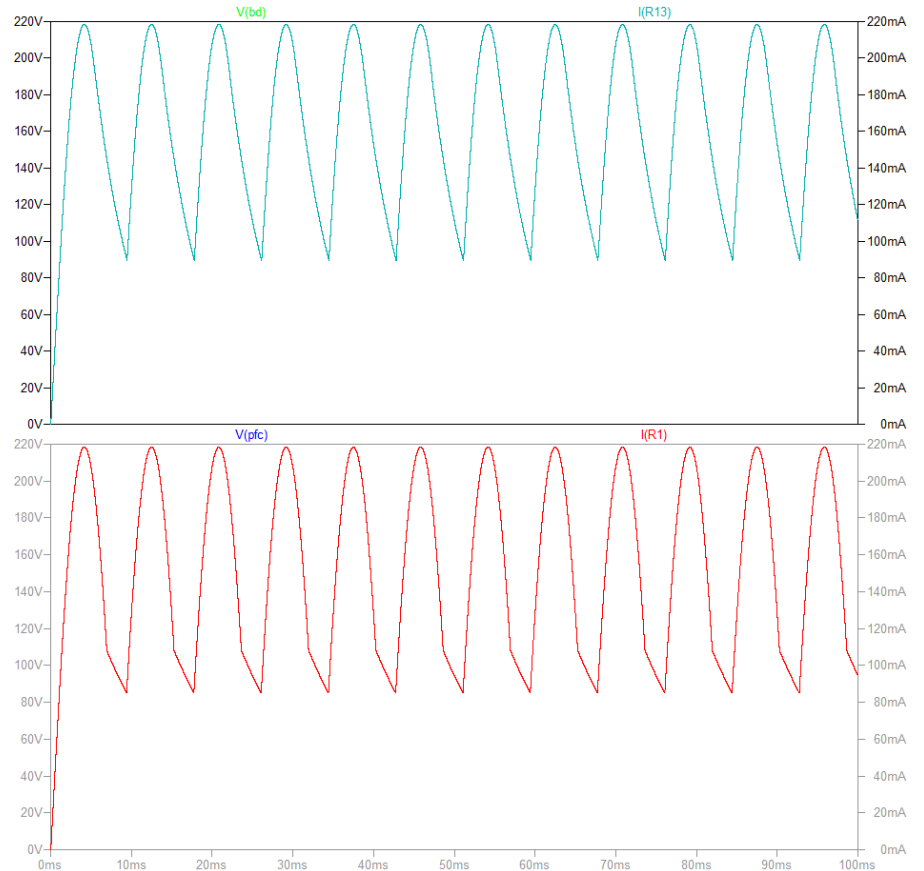

Figure 1 : Original valley-fill author by Spangler in 1988

$$C_{TOTAL} = \frac{\dfrac{P_{out}}{V_{(min)}} \times t_{HOLD}}{V_{DROOP}} = \frac{\dfrac{12.96\ W}{60\ V} \times 2.77\ ms}{20\ V} = 30\mu F$$

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TRADITIONAL RECTIFIER RIPPLES

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NOVEL TOPOLOGY OF SOLID STATE CAP FUNCTION BLOCK

AC INPUT → Rectifier → PFC/Charge → Dis-charge → **+VOUT**

Zero Current Detector → Charge and PF controller → PFC/Charge

Dis-charge controller → Dis-charge

Charge and PF controller ↔ Dis-charge controller
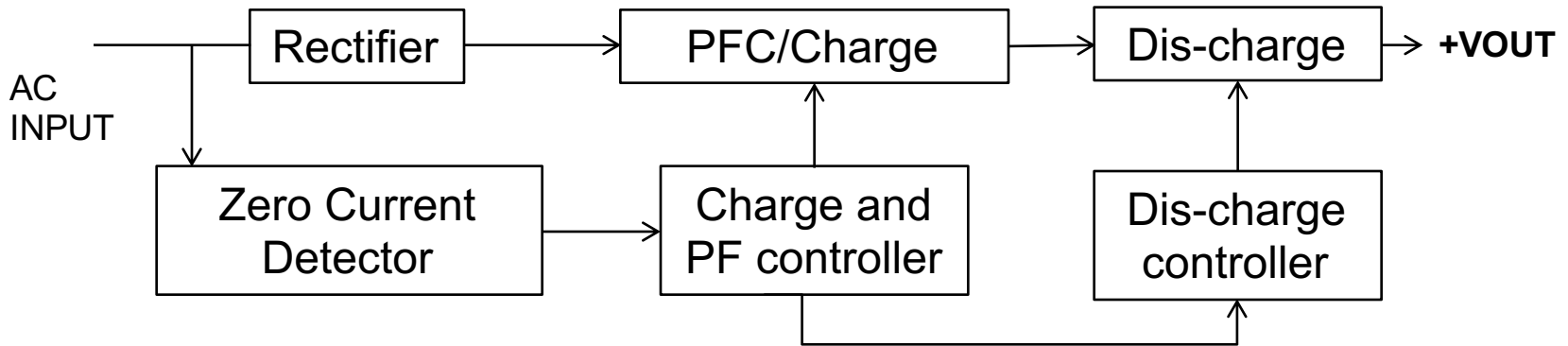
The PFC charger generates are valley fill voltage depend on discharge capacitors capacity. Reduce capacitance then needs to boost up then a p-p boost voltages. It's changed soft CCM to CCM or CrM mode of PFC.

*See the page 20 PFC simulation results.

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DIGITAL CAPACITOR BLOCK DIAGRAM

[AC-DC DIGITAL CAPACITOR]

DC OUT

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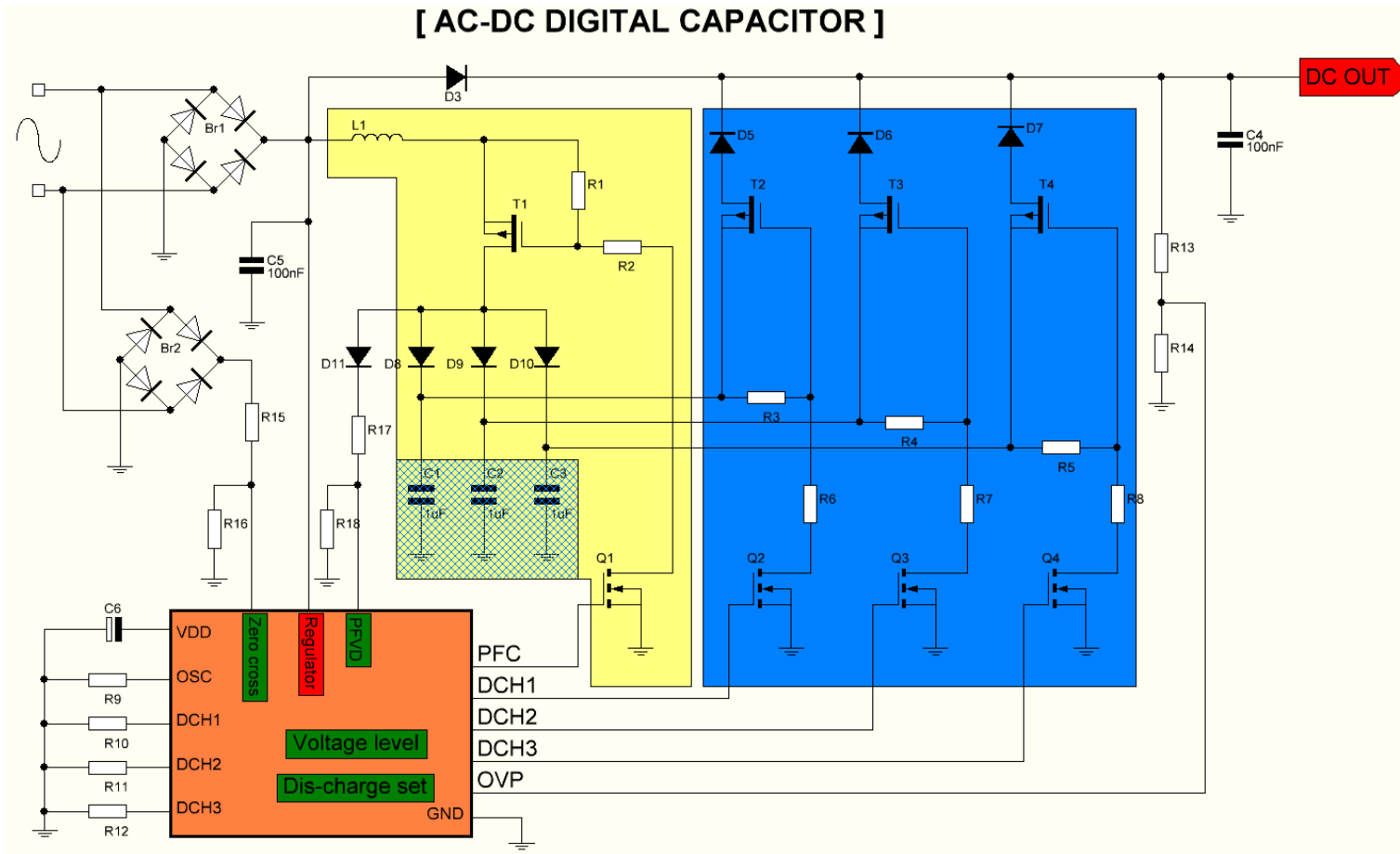
IK99XX용 MCM일례
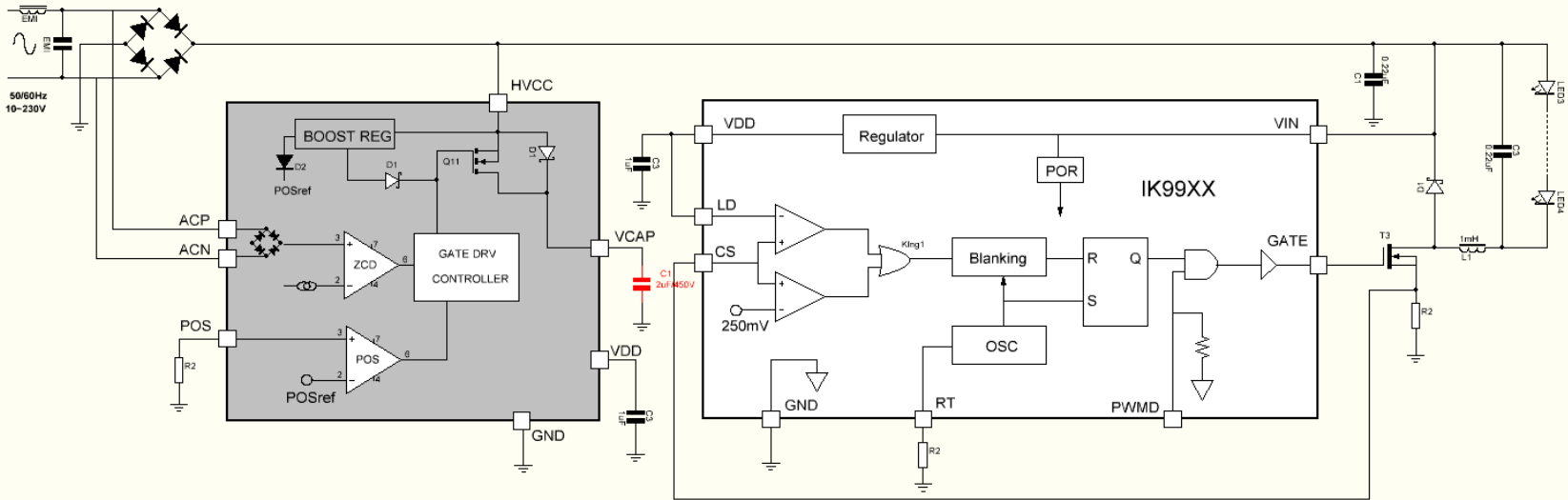
타사 대비 전해콘덴서 없이 리플을 완전히 제거 하고 PF는 0.85이상
(Soft Booster을 안 넣은 경우) Flyback방식의 전원에도 적용가능
내부 전원을 IK99xx에서 가져 오지 못할 경우 내부에 전원회로를 따로
설계해야 함.

PIN	기능	동작설명
POS	Resistor	방전위치 결정저항
VCAP	Vally Fill	Vally Fill용 고압 세라믹콘덴서
ACP,ACN	AC INPUT	제로크로싱검출 및 전압검출

17

ONE CHANNEL VALLY FILL
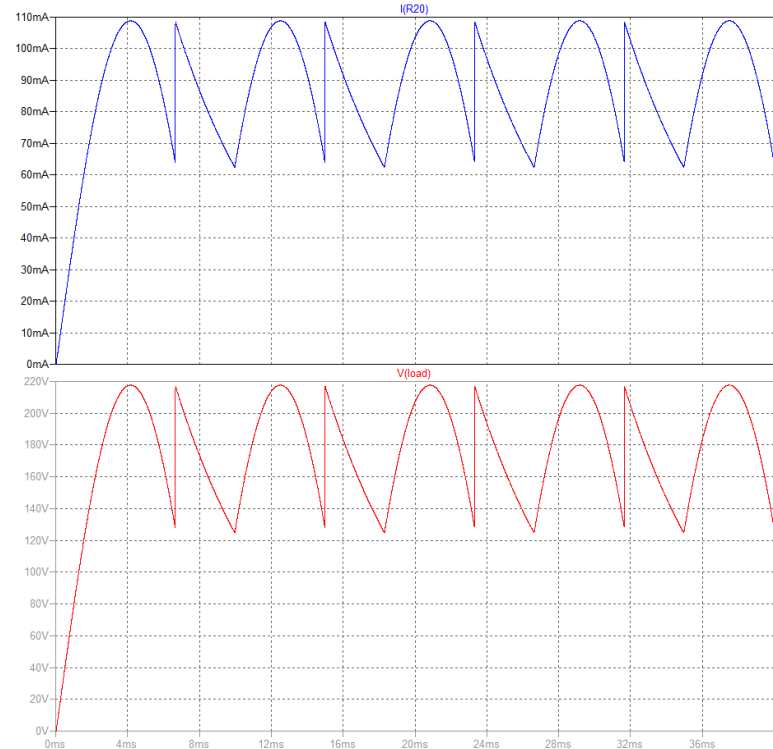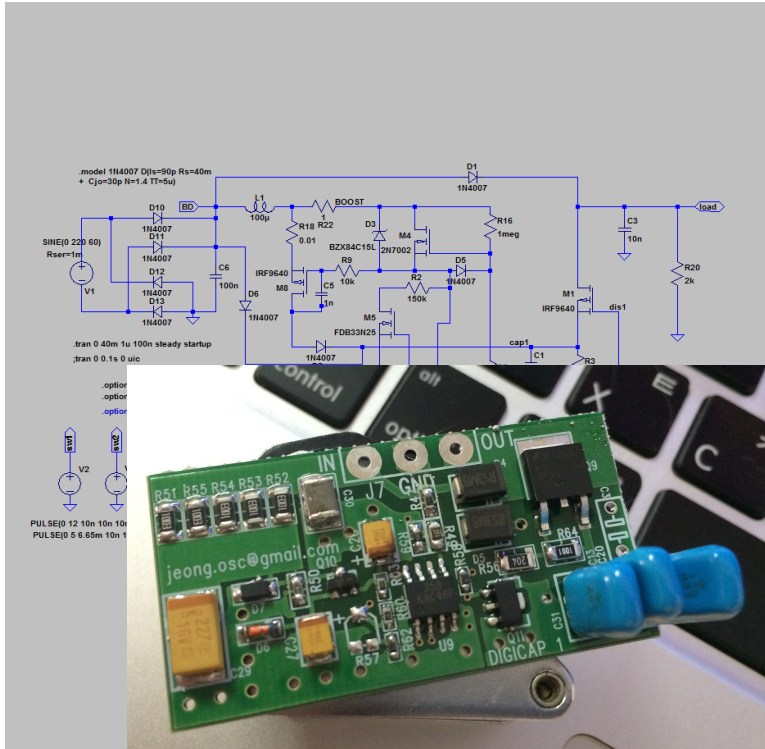
HV PROCESS IC특징 A
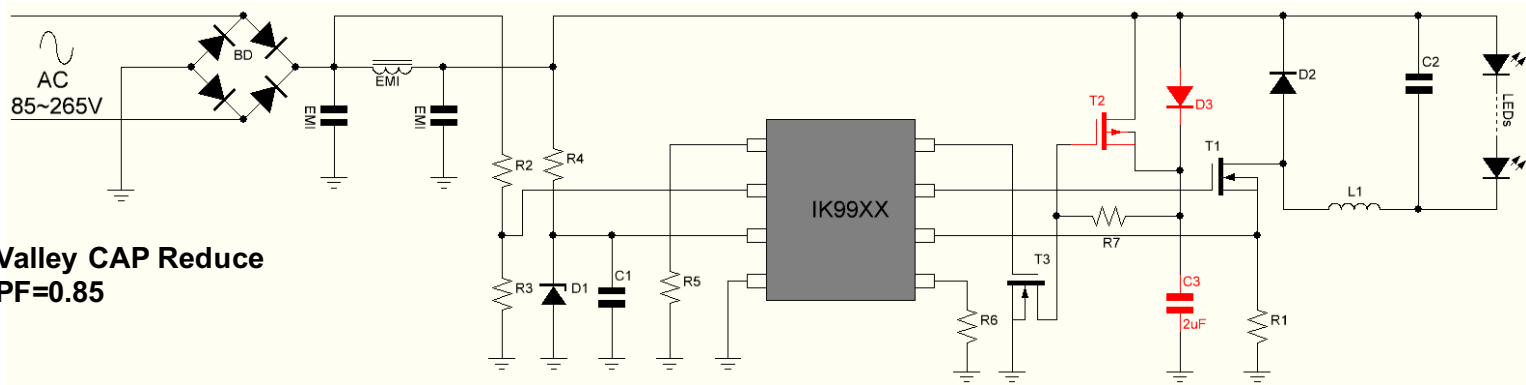
**Valley CAP Reduce
PF=0.85**

부품번호	상품명	동작설명
IK99xx	신규개발 IC	LED전원제어용
BD	Bridge Diode	AC전압의 전파정류
EMI L,C	세라믹, 인덕터	복사노이즈제거용
R2, R3	1/8W저항	AC전압검출용
R4, C1, D1		IC용 정전압회로
D2	Shortky Diode	Flyback용
T1	Power MOS FET	Buck용 TR
T2,T3, D3, C3	Valley Fill 용 고압세라믹콘덴서 및 드라이버	부하에 따라 1~3uF
R6	On/Off Dimming	On/Off 및 Dimmg 설정저항
R5	Discharge Voltage Set	Valley Fill세라믹 콘덴서방전시간설정

HV PROCESS IC특징 B
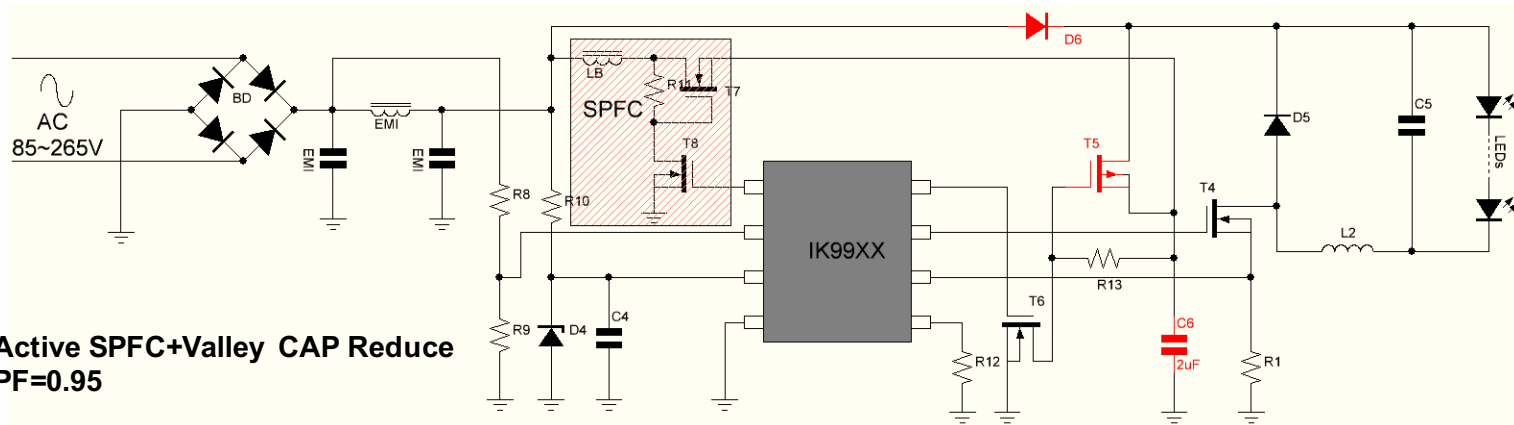
Active SPFC+Valley CAP Reduce PF=0.95

부품번호	상품명	동작설명
IK99xx	신규개발 IC	LED전원제어용
BD	Bridge Diode	AC전압의 전파정류
EMI L,C	세라믹, 인덕터	복사노이즈제거용
R8, R9	1/8W저항	AC전압검출용
R10, C4, D4		IC용 정전압회로
D6	Shortky Diode	Flyback용
T4	Power MOS FET	Buck용 TR
T5, D6, C6	Valley Fill 용 고압세라믹콘덴서 및 드라이버	부하에 따라 1~3uF
R12	On/Off Dimming	On/Off 및 Dimmg 설정저항
SPFC	PFC+Valley Fill Booster	Valley Fill세라믹 콘덴서용량저감

REGULATION RIPPLE COMPARED

The all circuits are AC 167V /60Hz at 2K load.

Reliability and size with costs incurring tremendously good.
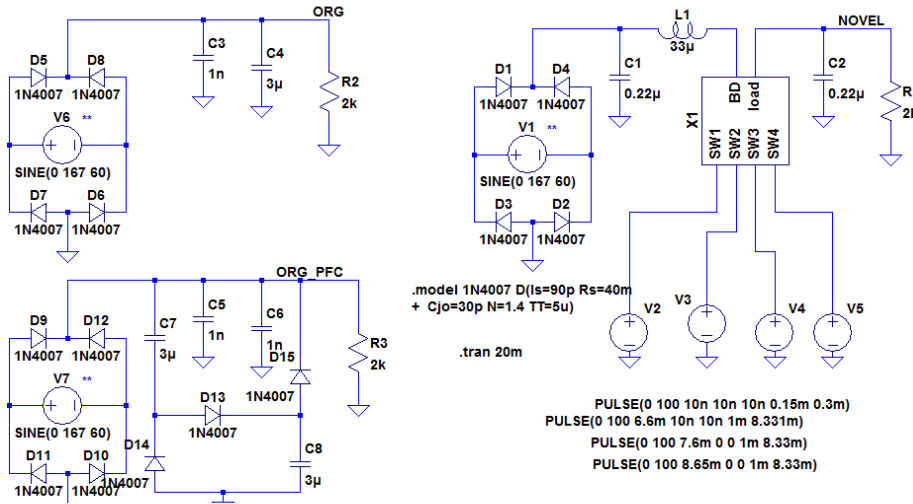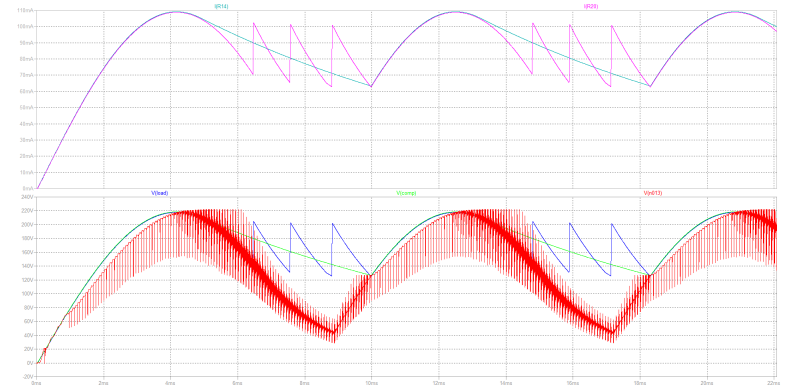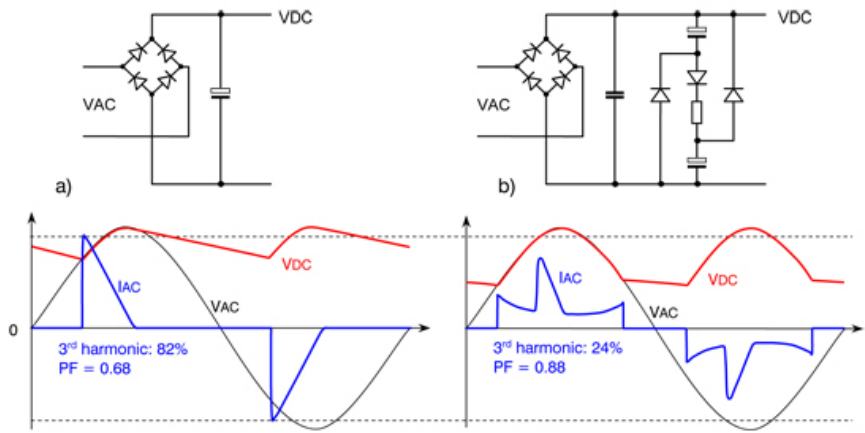
SOLID STATE VALLEY FILL WITH PF CORRECTION TOPOLOGY

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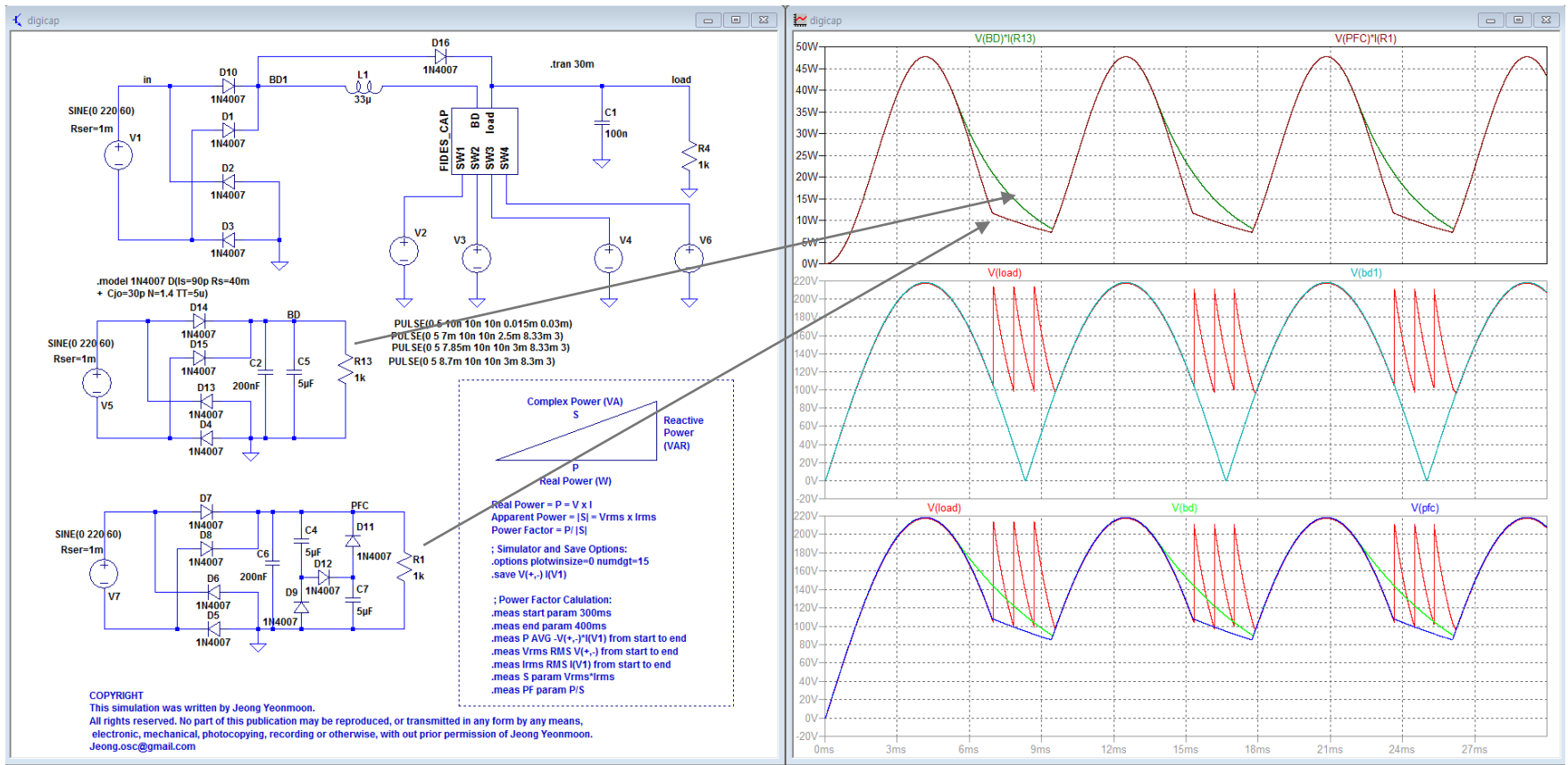
DIGITAL CAPACITOR WAVE FORM

220V/60Hz   5uF

LOAD=2K

1uFx3

Boost V setting are
depending on charge cap
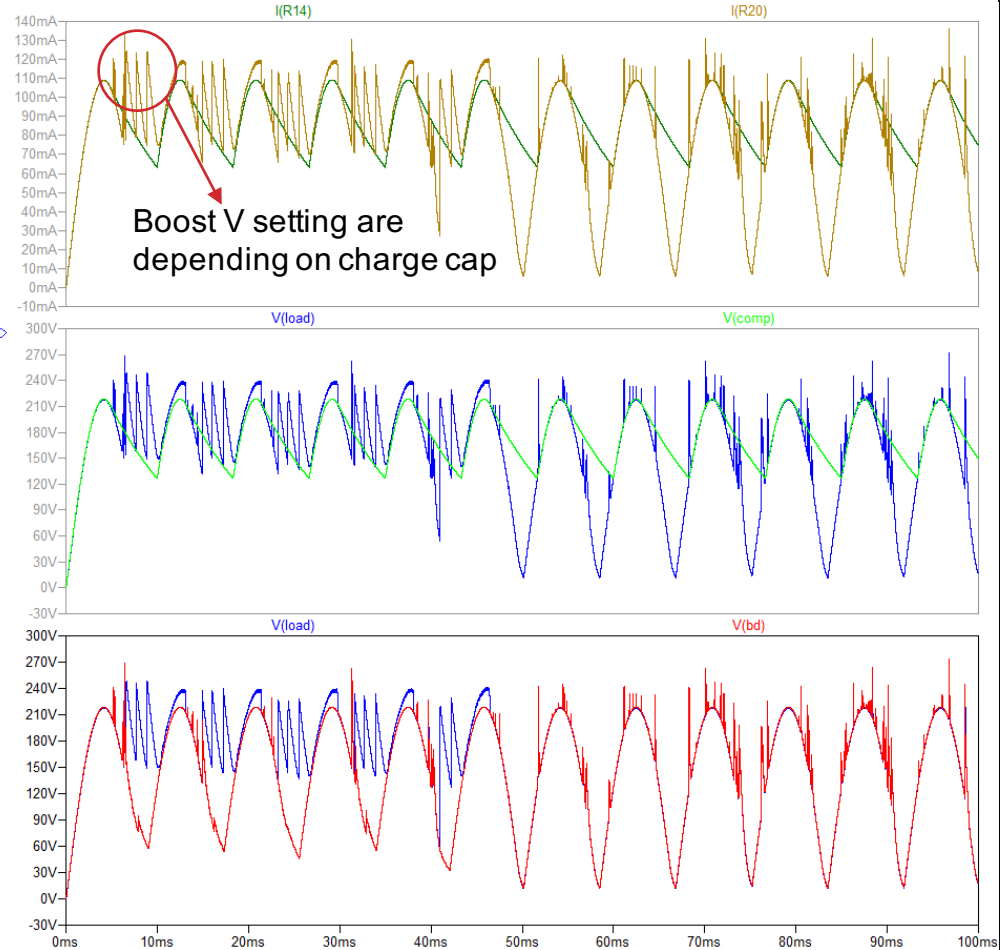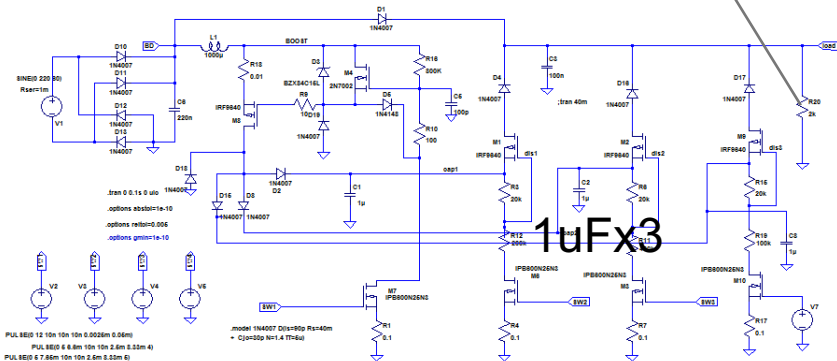
AC220V/60Hz LOAD=2K
Ordinary rectifier ECAP are 5uF

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SINGLE PHASE BOOST PFC CONVERTER USING HYSTERESIS CURRENT MODE CONTROL TECHNIQUE
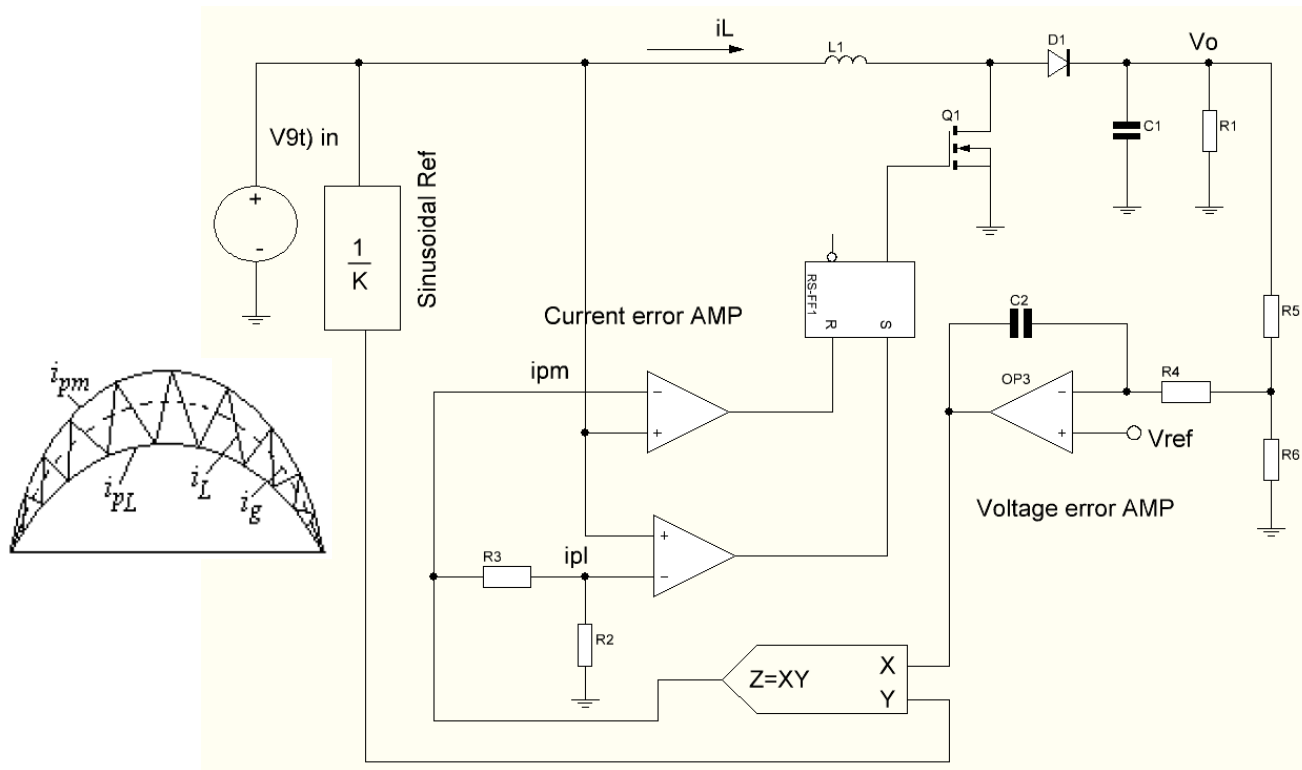
Hysteresis comparators are used to impose hysteresis band around the reference current. The hysteresis control scheme provides excellent dynamic performance because it acts quickly.

Also, an inherent peak current limiting capability is provided. This type of control in which two sinusoidal current references *ipm*, *ipL* is generated corresponding to maximum and minimum boundary limits.

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ADVANCED SOFT SWITCHING PFC EXAMPLES
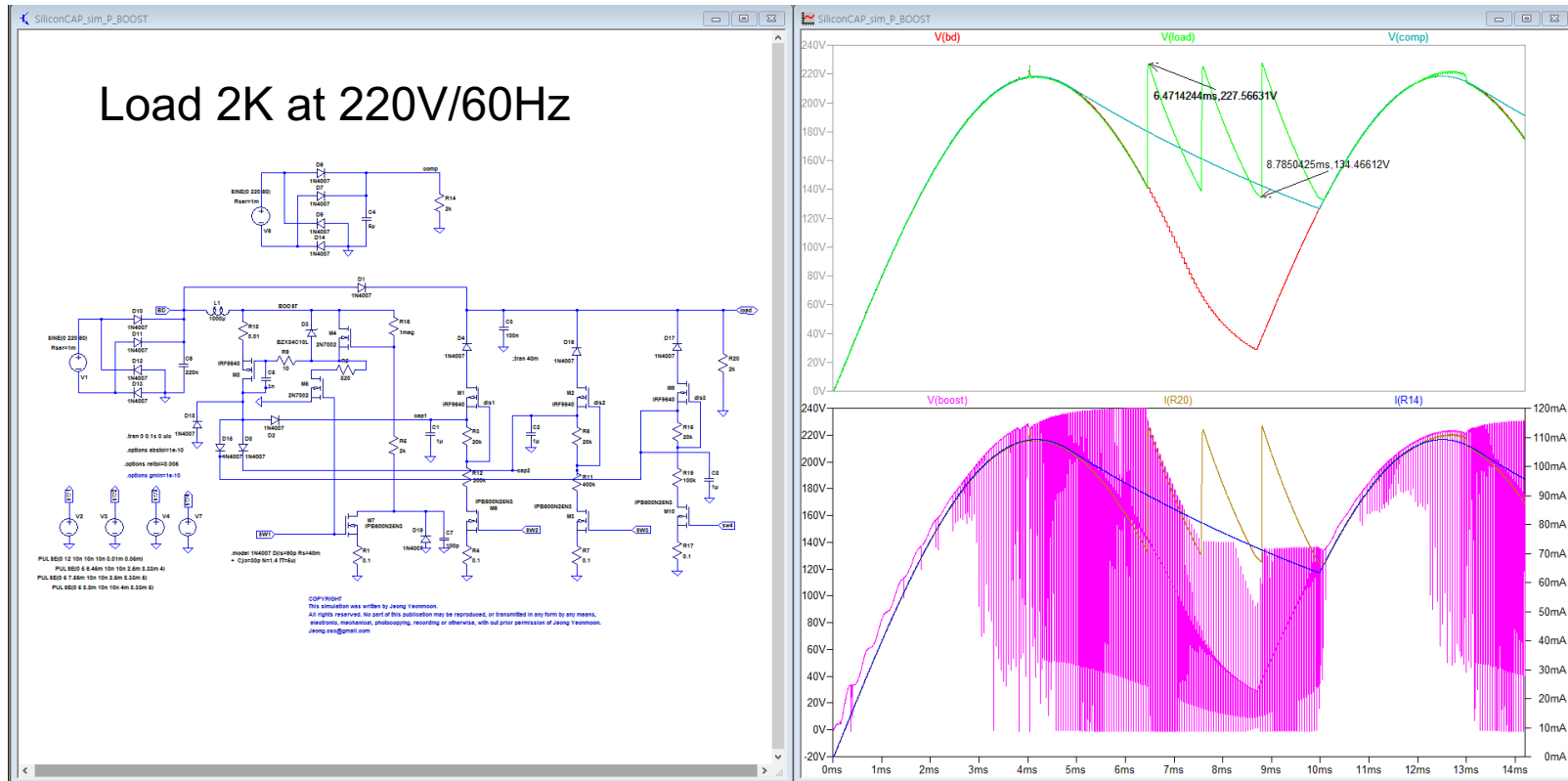
The soft-switching PFC technique combines the advantages of PWM mode and resonant mode techniques with an additional resonant network consisting of a resonant inductor, a resonant capacitor and an auxiliary switch. The AC/DC converter operates in PWM mode during the most portion of a switching cycle but operates in resonant mode during the switch turn-on and turn-off intervals. As a result, the PFC circuit works at the constant switching frequency and the power switch turns on and off at zero current or zero voltage conditions. Thus, efficiency and power factor both improved by this technique. This figure shows boost PFC circuit with a soft switching network

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CHANGED PFC BOOSTING VALUES

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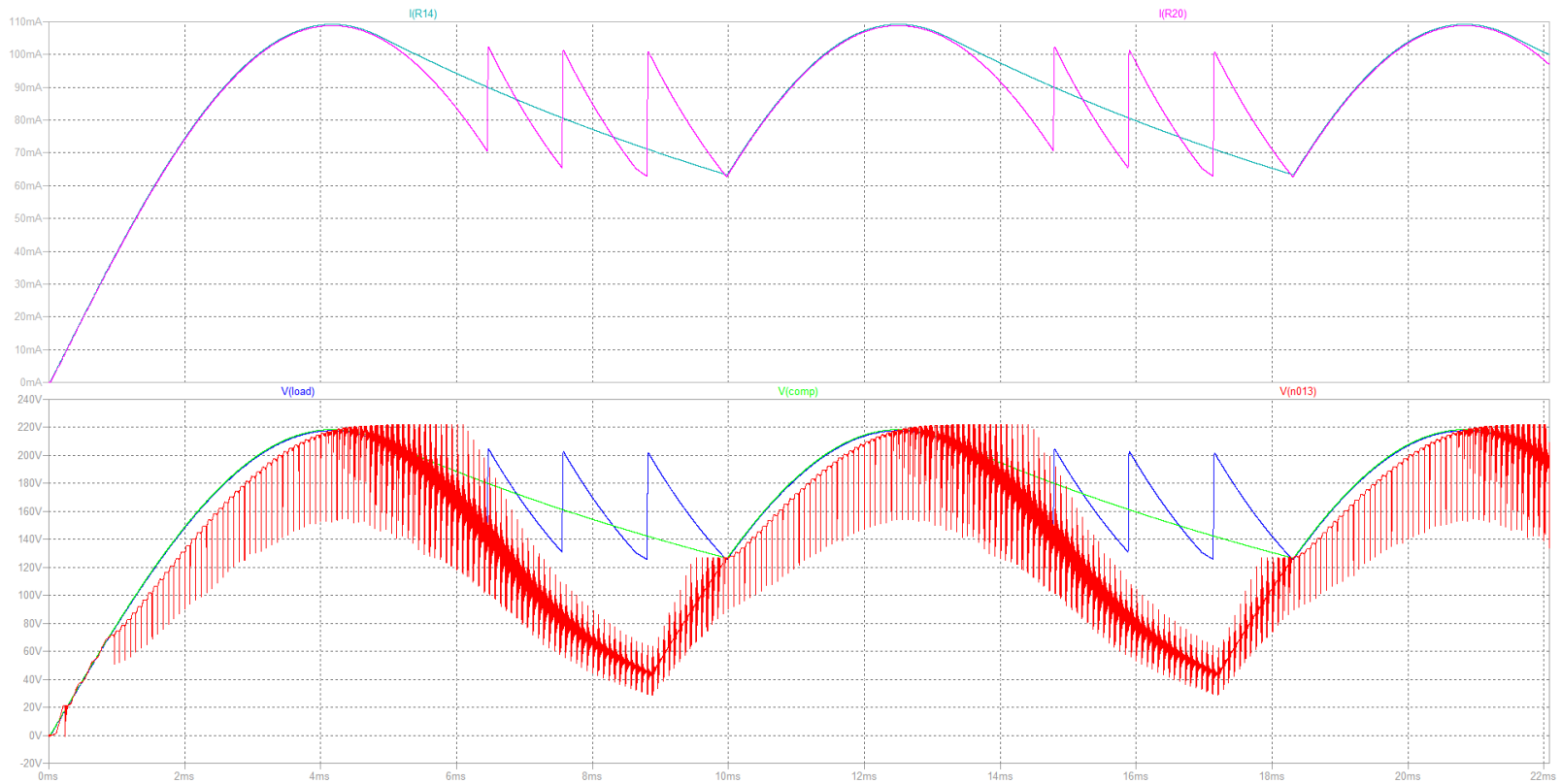
NOVEL SOLID STATE VALLEY FILL RECTIFIER
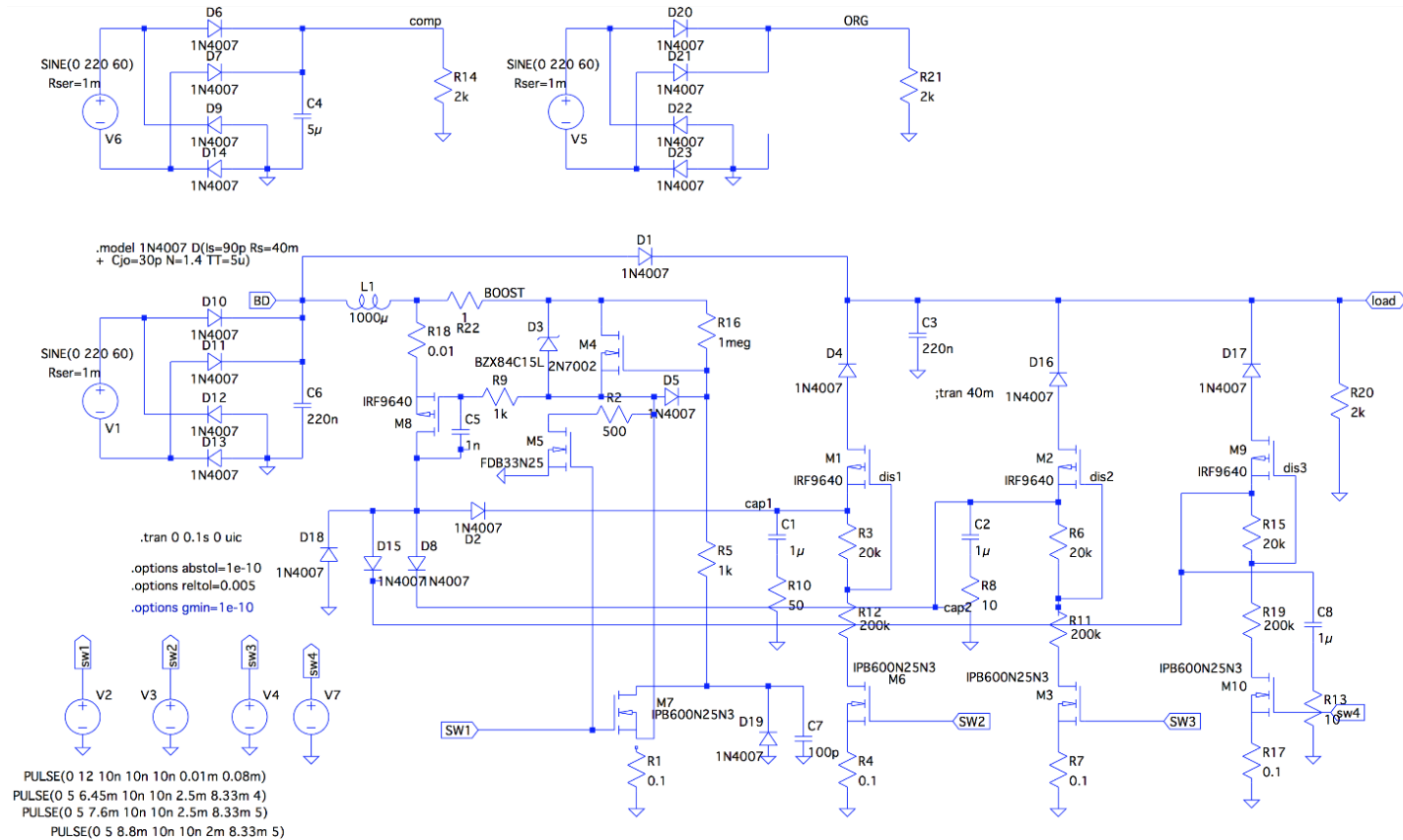
Jeong.osc@gmail.com

COMPARED SIMULATION RESULTS
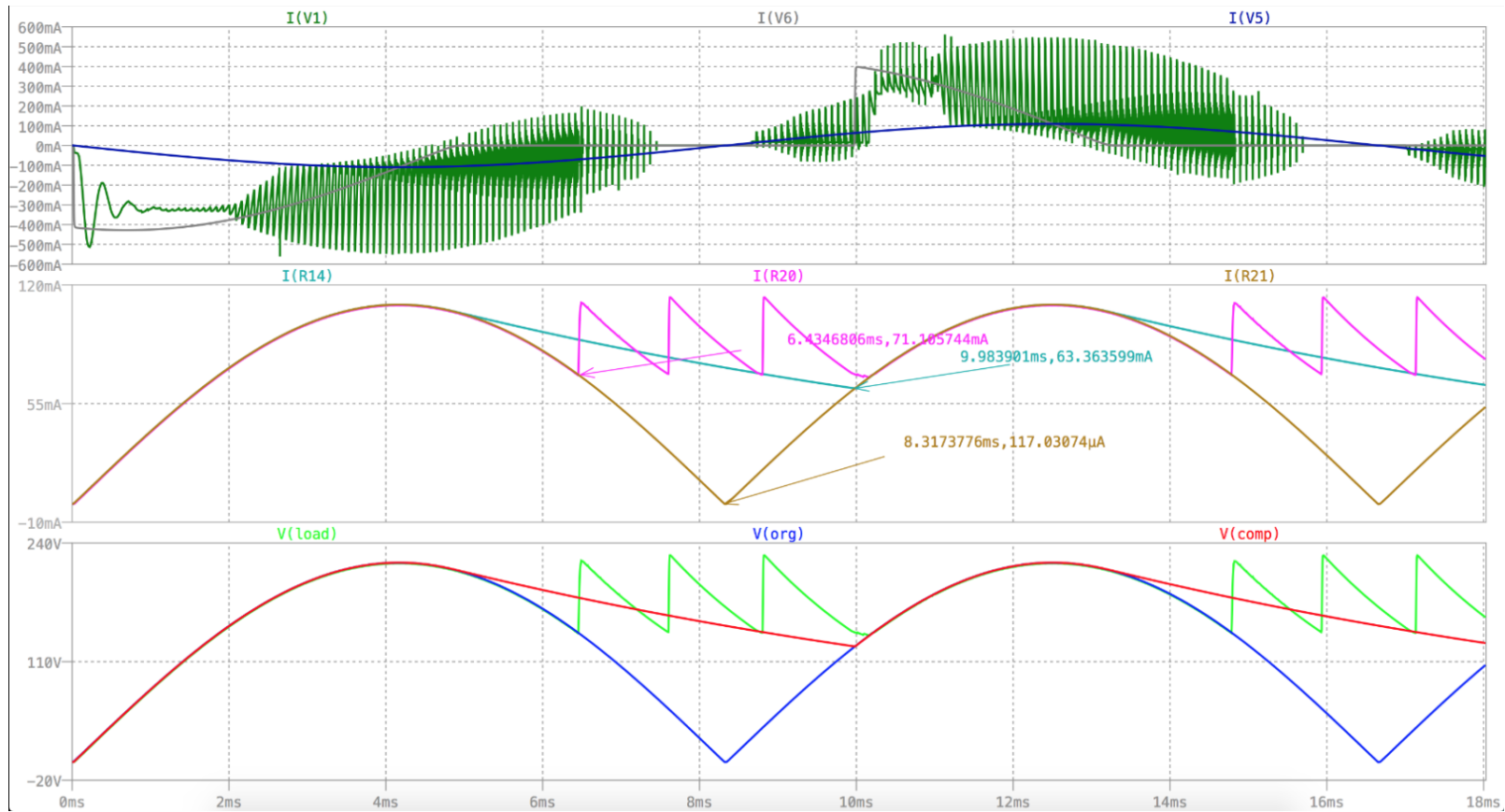
Jeong.osc@gmail.com

FFT COMPARE OF AC INPUT
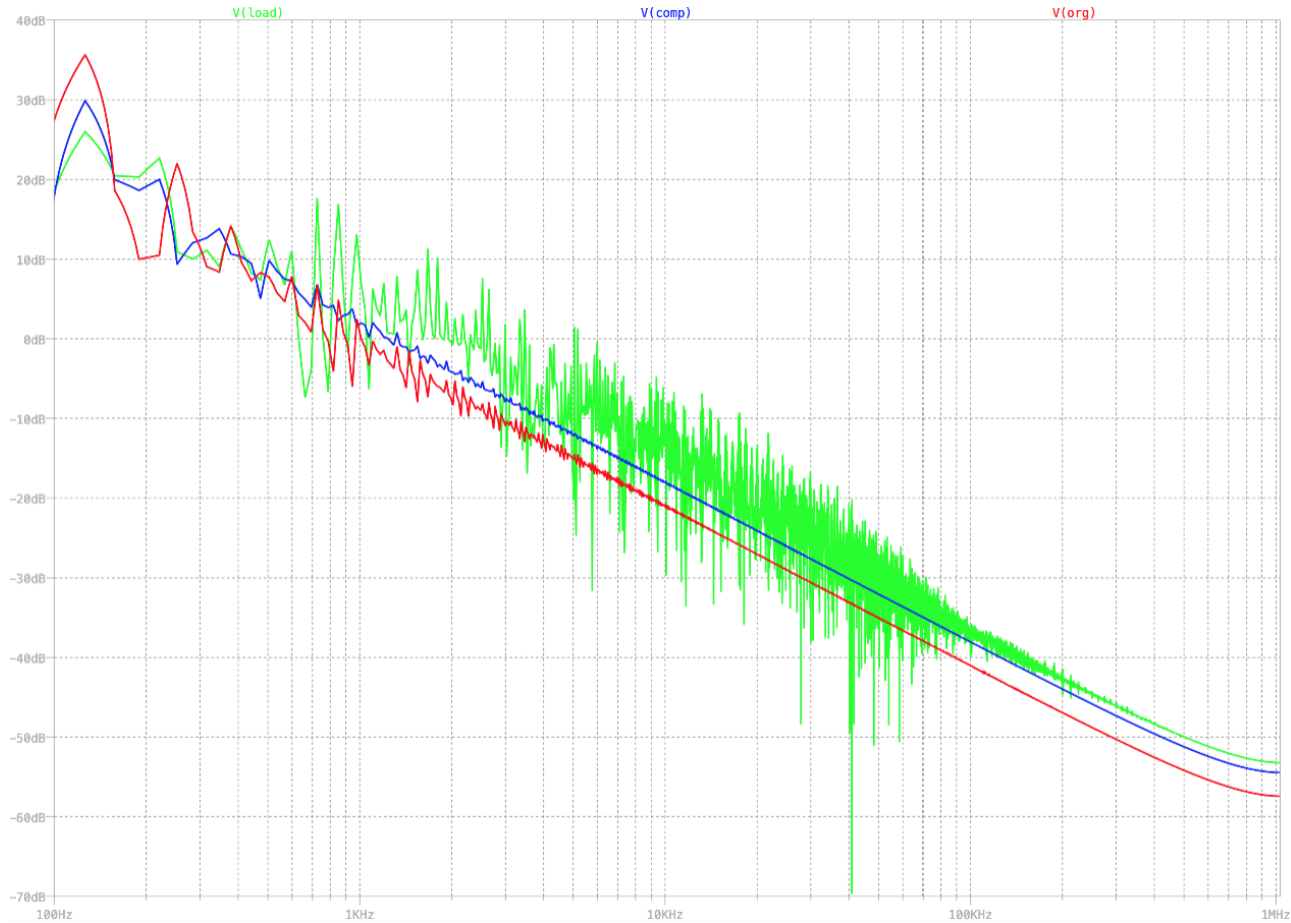
Jeong.osc@gmail.com

ONSEMI NXP101X WITH DIGICAP
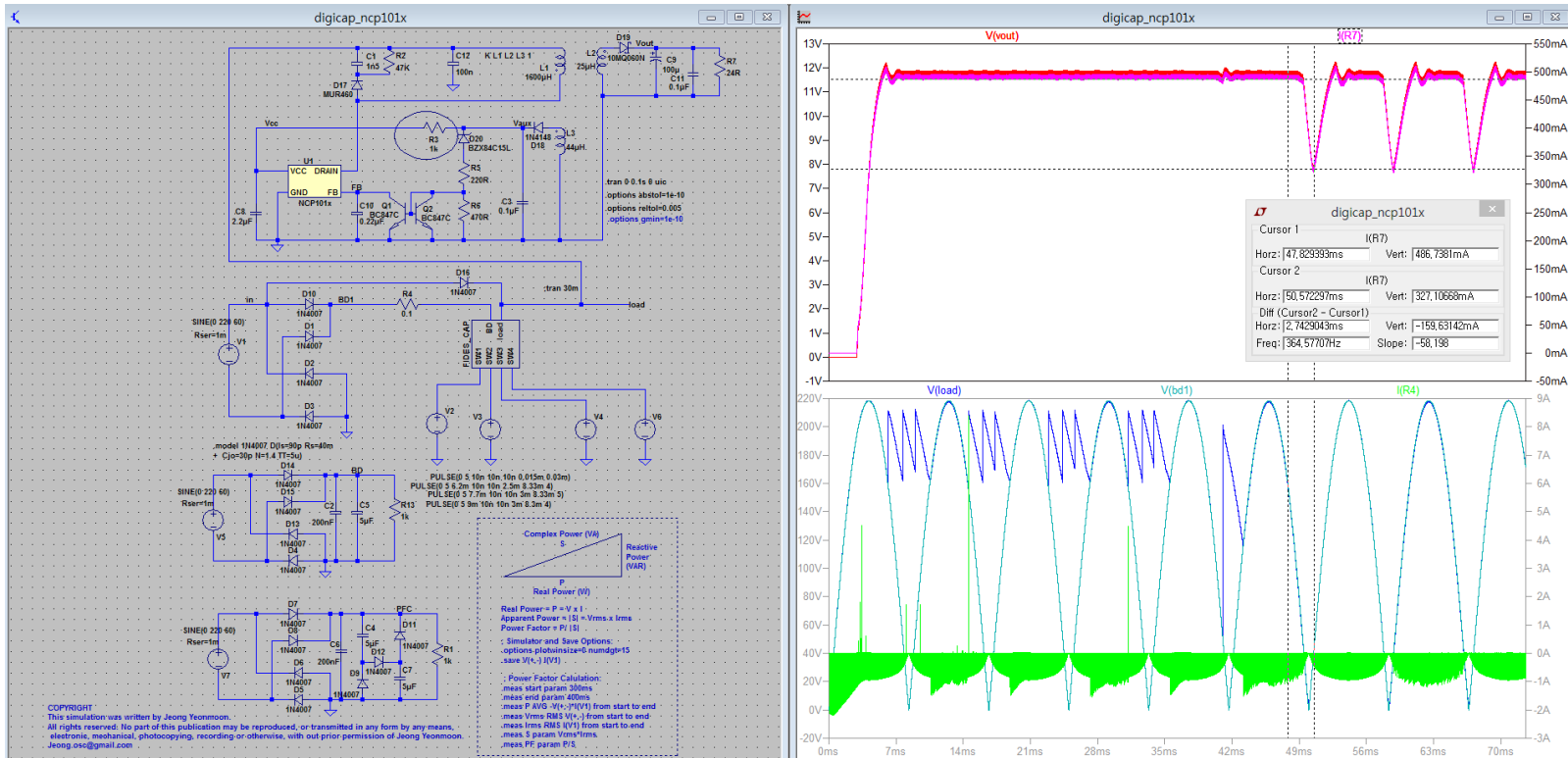
Jeong.osc@gmail.com

OVERLOAD RIPPLE COMPARE
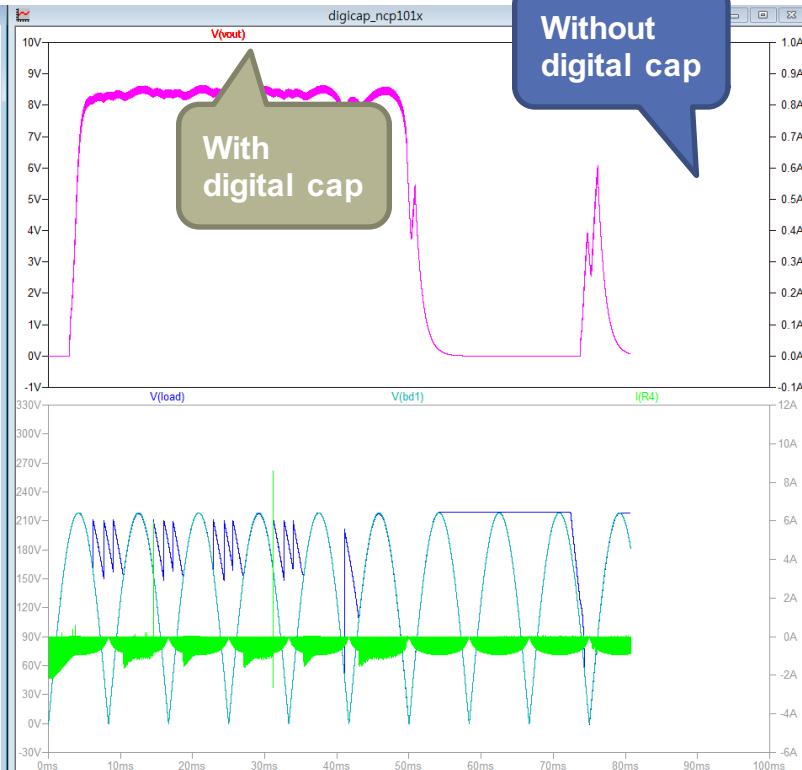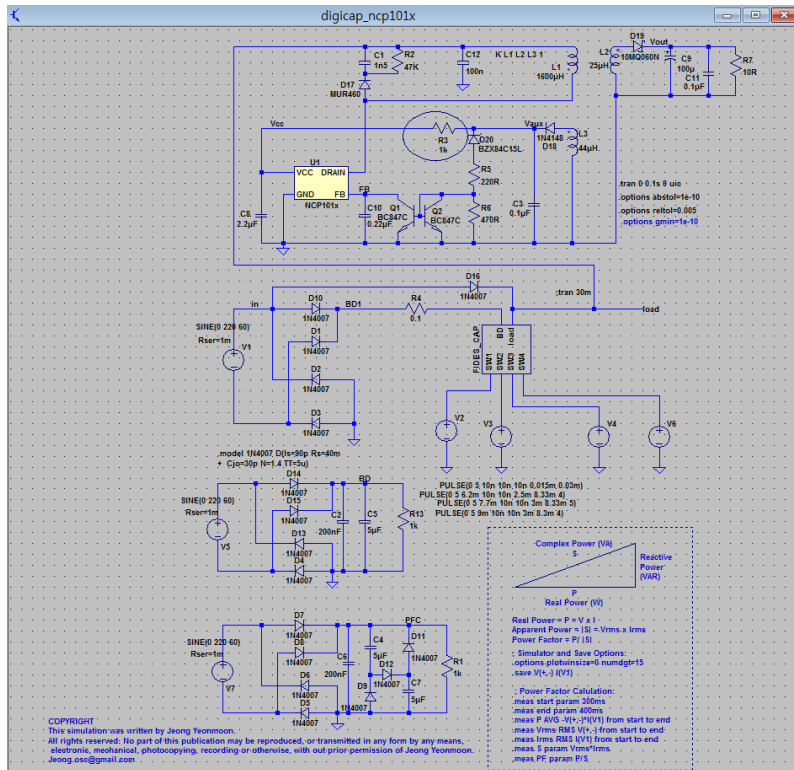
Jeong.osc@gmail.com

ORDINARY SMPS OVERLOAD CONDITION

Ordinary technology can not sustain to overload condition
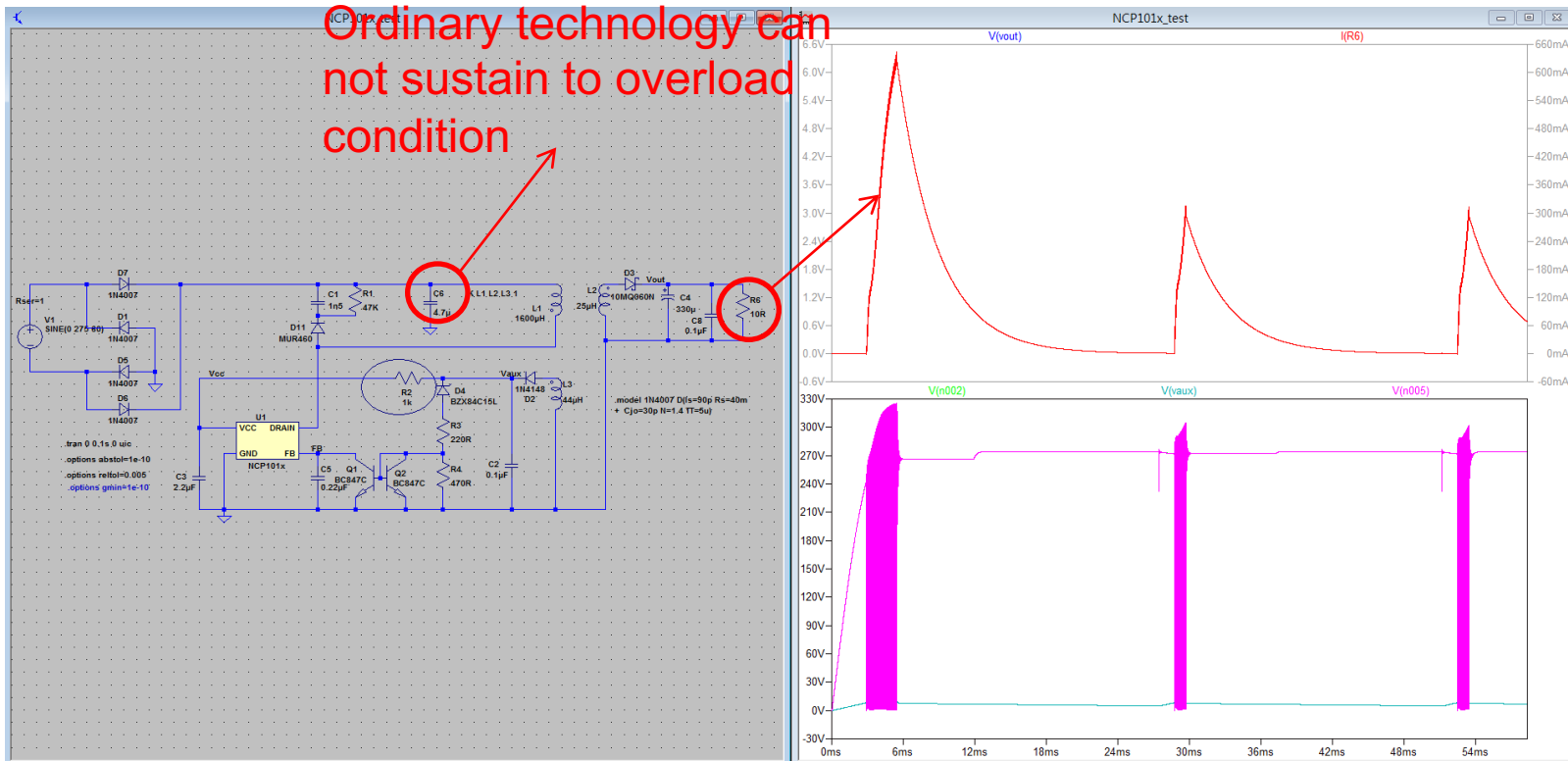
Jeong.osc@gmail.com

FIDES-DIGICAP DEMO

HV9910B

113.2mm
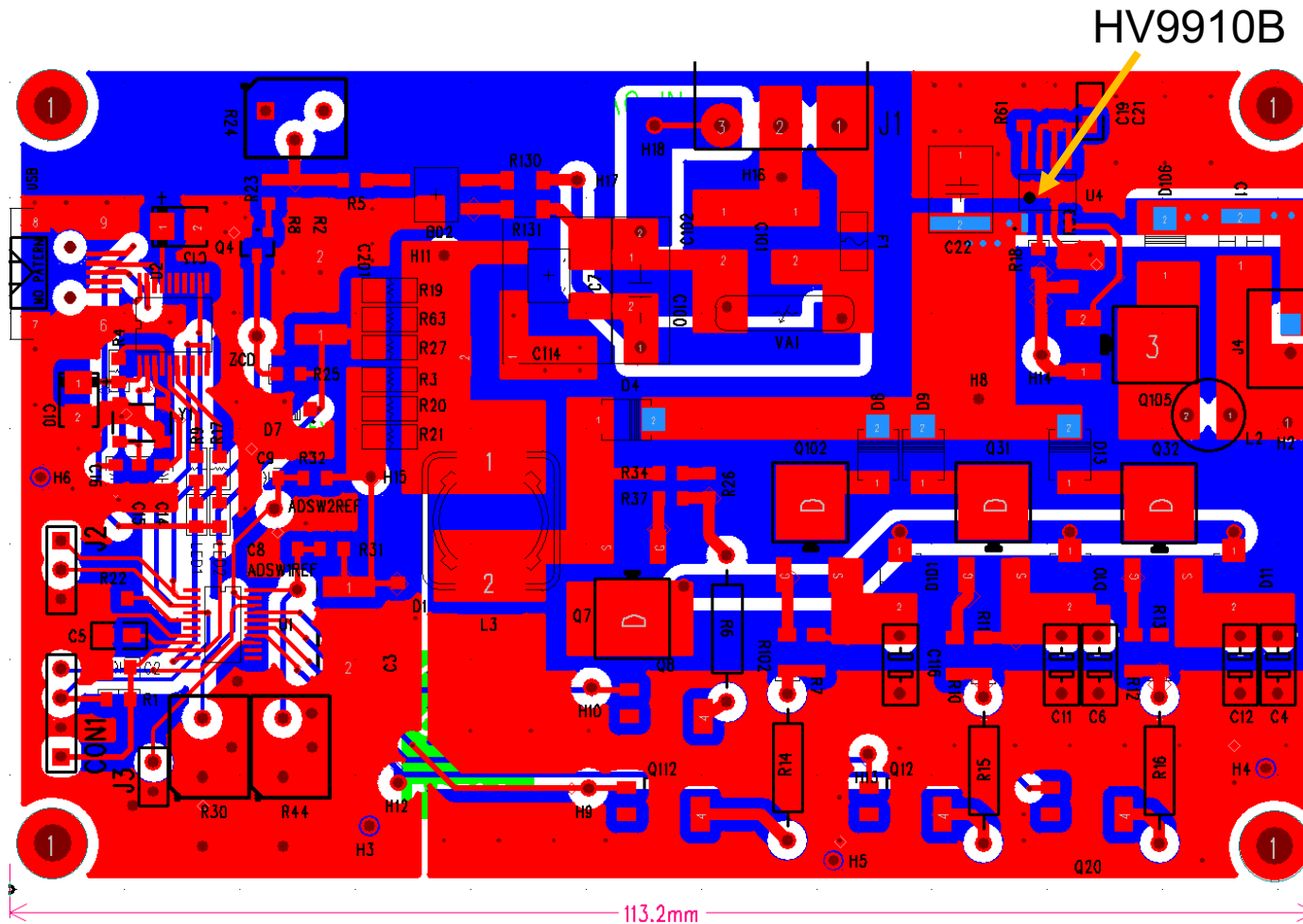
HV9910B + SILICON CAP DEMO (LOAD LED16W)
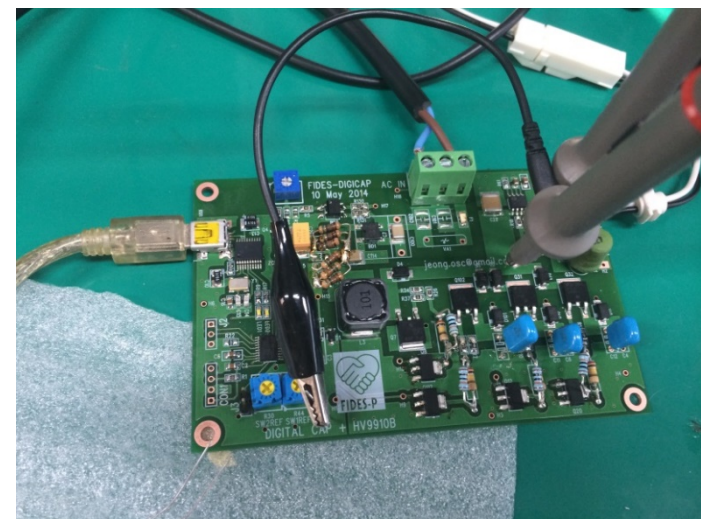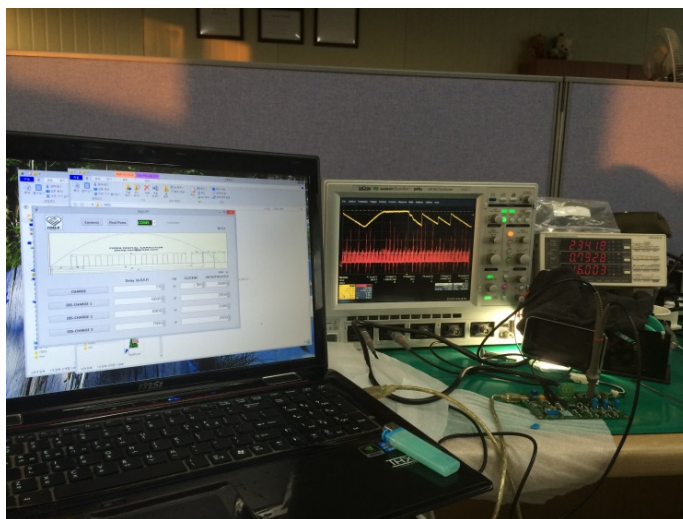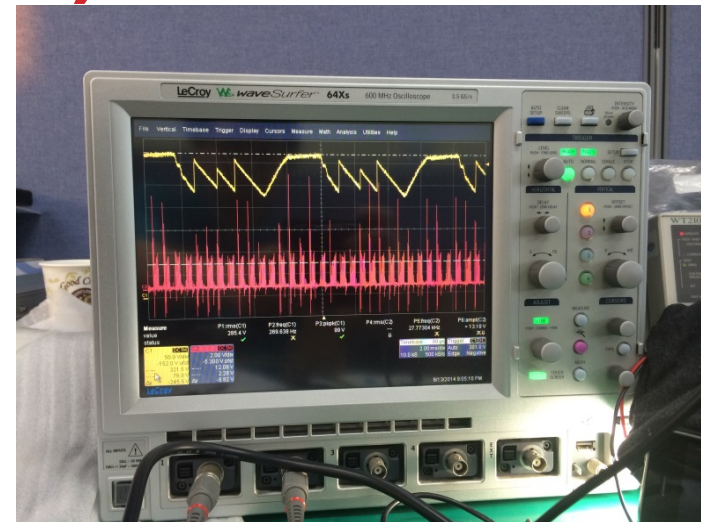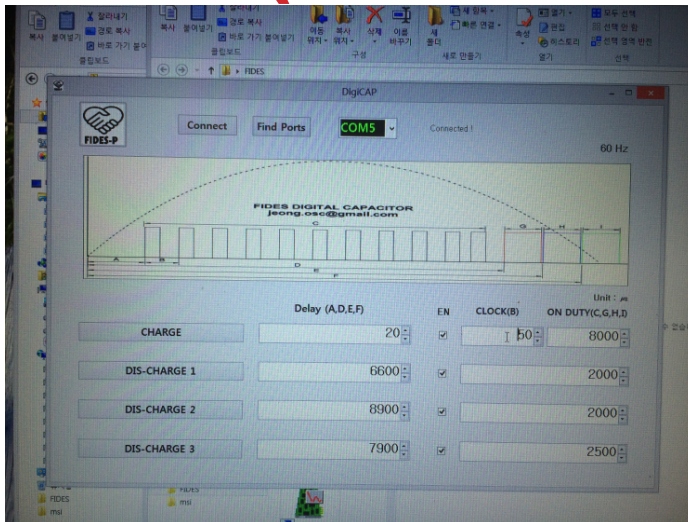
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ANY QUESTIONS?

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